G 2953 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JULY 2010

First Semester

Specialization : VLSI and Embedded Systems

Branch : Electronics and Communication Engineering

LMV-101—ANALOG INTEGRATED CIRCUIT DESIGN

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions, each carries* 4 *marks.*

1. Explain the factors of fixing the threshold voltage of a MOS transistor.
2. Draw the small signal MOSFET equivalent circuit with body effect current source and explain.
3. With a neat circuit diagram, explain the advantages of a regulated cascade mirror.
4. What are active CMOS loads ? Explain their advantages and applications.
5. Define and explain the common mode range (CMR) of a CMOS op-amp.
6. With the help of graphs, describe the common mode voltage transfer characteristics of CMOS differential amplifier.
7. What is the maximum possible value of β using resistors in the feedback loop of a noninverting op-amp circuit ? Sketch this op-amp circuit when $\beta = \frac{1}{2}$.
8. How the gain margin and phase margin can be used to determine stability ?

(5 × 4 = 20 marks)

Part B

Answer **all** *questions, each carries* 20 *marks.*

9. (a) Sketch and explain the noise model for MOSFET. (10 marks)

   (b) Discuss the effect of temperature on the parameters of MOSFET. (10 marks)

Or

10. (a) Sketch to scale the output characteristics of an enhancement *n*-channel device if $V_T = 0.7$ V and $I_D = 500\ \mu A$ when $V_{GS} = 5V$ in saturation. Choose values of $V_{GS} = 1, 2, 3$ and 4V. Assume that the channel modulation parameter is zero.

(10 marks)

(b) With the help of neat sketches, derive the expressions for the drain current in triode region for an N-channel MOSFET considering the velocity saturation of carriers due to large electric fields.

(10 marks)

Turn over

11. (a) What is the basic principle of a current mirror ? How it is used in a CMOS circuit ? Explain its applications.

(10 marks)

(b) With a neat circuit diagram describe the principle of a folded cascode structure. What are its merits ?

(10 marks)

Or

12. With a circuit diagram, show how a current mirror can be used as an active load. Derive the expressions for the voltage gain, input resistance and output resistance of a common source amplifier using such an active load.

(20 marks)

13. (a) Show that if the voltage gain of an op-amp approaches infinity, the differential input becomes a null port. Assume that the output is returned to the input by means of negative feedback.

(10 marks)

(b) For an op-amp model with two poles and one RHP zero, prove that if the zero is ten times larger than GB, then in order to achieve a 45° phase margin, the second pole must be placed at least 1.22 times higher than GB.

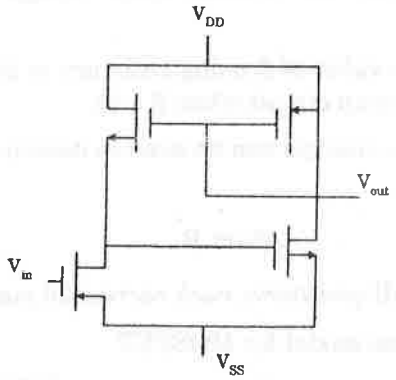
(10 marks)

Or

14. Draw the complete internal circuit diagram of a low voltage, two stage CMOS op-amp and explain each stage in it. Describe the performance of any five important parameters of the circuit.

(20 marks)

15. (a)



A MOS output stage is shown in Fig. Draw a small signal model and calculate the ac voltage gain at low frequency. Assume that bulk effects can be neglected.

(10 marks)

(b) Draw and explain the circuit diagram of a two-stage Miller differential-in and differential-out op-amp with common-mode stabilization.

(10 marks)

Or

16. (a) With neat circuit diagram, explain the frequency compensation in a two-stage CMOS op-amp showing its bode plots of loop gain.

(10 marks)

(b) With necessary circuit diagrams, show how the mismatch in MOS differential circuits can be reduced.

(10 marks)

[4 × 20 = 80 marks]

G 2954 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JULY 2010

First Semester

Specialization : VLSI and Embedded Systems

Branch : Electronics and Communication Engineering

LMV-102—CMOS DIGITAL INTEGRATED CIRCUITS

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions, each carries* 4 *marks.*

1. Discuss the rules governing minimum layout spacings.
2. Realise $Y = \overline{(A + B(C + DE))}$ using NMOS transistors.
3. What is stick diagram ? State its role in the fabrication of ICs.
4. Draw and explain the operation of CMOS transmission gates.
5. Design CMOS logic gates for the following :—

$$Z = \overline{(A \cdot B + C \cdot (A + B)}.$$

6. Use a combination of CMOS gates to generate :

$$Z = A \cdot \overline{B} + \overline{A} \cdot B \text{ (XOR)}.$$

7. Design a 2 : 4 decoder defined by

$$Z = \overline{A}_0 \cdot \overline{A}_1.$$

8. Does the body effect of a process limit the number of transistors that can be placed in series in a CMOS gate at low frequencies ?

(5 × 4 = 20 marks)

Part B

Answer **all** *questions, each carries* 20 *marks.*

9. (a) Draw neatly the layout of a n-MOS transistor in a *p*-well process having action *p*-select, *n*-select, polysilicon, contact and metal 1 masks. Include the well contact to V_{DD}.

(14 marks)

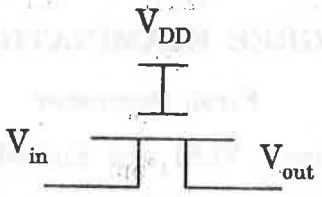
(b) Compare and contrast between the first order and second order effects scaling of MOS transistors.

(6 marks)

Or

Turn over

10. (a) If V_{DD} = 1.2 V, V_t = 0.4 V. Determine V_{out} for (i) V_{in} = 0 V, (ii) V_{in} = 0.6 V, (iii) V_{in} = 1.2 V. Neglect body effect for the Fig shown below :



(10 marks)

(b) Sketch the stick diagram of a CMOS inverter. (10 marks)

11. (a) Explain the importance of substrate and well contacts in CMOS. (10 marks)

(b) What is the best possible metal for interconnect ? Why isn't it used ? (4 marks)

(c) How might you use a field transistor to prevent overvoltage in a CMOS chip ? (6 marks)

Or

12. (a) Find the worst case Elmove parasitic delay of a *n*-input NOR gate. (10 marks)

(b) A three-stage logic path is designed so that the effort borne by each stage is 12, 6 and 9 delay unit respectively. Can this design be improved ? Why ? What is the best number of stages for this path ? What changes do you recommend to the existing design ?

(10 marks)

13. (a) Find the input and output logic levels and high and low noise margins for an inverter with a 3 : 1 P/N ratio. What P/N ratio maximizes the smaller of the two noise margins for an inverter ?

(10 marks)

(b) Explain how you might estimate and plan the clock distribution scheme in a chip. Summarize the paremeters that are relevant and show how your scheme deals with these.

(10 marks)

Or

14. (a) For a pseudo-nMOS inverter,

(i) What V_{OL} must be chosen such that the pull down transistor of a subsequent pseudo-nMOS gate will be off when the inverter's output is logic 1 ?

(ii) What is the ratio $W_P/L_p/W_n/L_n$ required to achieve this output voltage ?

(10 marks)

(b) Draw a stick diagram for a two-input multiplexed latch. Place the two transmission gates side-by-side.

(10 marks)

15. Produce a complete table of the barrel shifter's possible operations. List all possible combinations of top and bottom inputs and the resulting operation. Identify the critical path delay through the barrel shifter.

(20 marks)

Or

16. Design components of a Booth multiplier :

(i) Design the logic for one bit of the adder-subtractor.

(ii) Design a stick diagram for your adder-subtractor.

(20 marks)

[4 × 20 = 80 marks]

G 2955 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JULY 2010

First Semester

Specialization : VLSI and Embedded Systems

Branch : Electronics and Communication Engineering

LMV-103—ADVANCED DIGITAL SYSTEM DESIGN

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions, each carries* 4 *marks.*

1. What are the causes of hazards in a combinational circuit ?
2. Distinguish between static-1 and static-0 hazard.
3. Explain why testing a sequential circuit is more difficult.
4. Give the architectural floor view of PLA.
5. Prove that dynamic hazards do not occur in two-level AND-OR and two-level OR-AND circuits.
6. Explain how FPGA can be reprogrammed.
7. Write down the precedence of all the operators in verilog.
8. Clearly explain bit swizzling.

(5 × 4 = 20 marks)

Part B

Answer **all** *questions, each carries* 20 *marks.*

9. (a) Explain sequential logic testing with an example. (5 marks)

   (b) Explain a method of testing used in BIST methodology. What are its merits and demerits ? (10 marks)

   (c) Explain the design for testability as applied to synchronous sequential circuits. What isa scan flip-flop ? (5 marks)

Or

10. (a) Is the single s-a-o fault shown in Fig.1 detectable ? If so, find the test vector using path sensitization method :

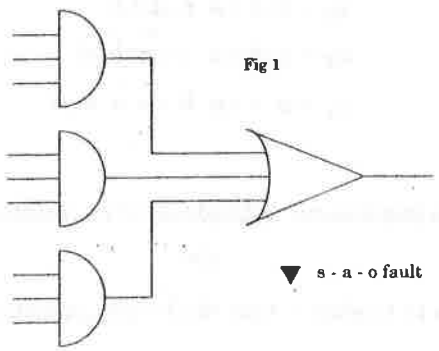


Fig 1

(15 marks)

Turn over

(b) Explain the different kinds of physical faults that can occur on a CMOS chip and relate them to typical circuit failures. (5 marks)

11. Detect the static hazard in a two-level circuit in Fig. 2 below. Obtain the corresponding hazard free circuit.

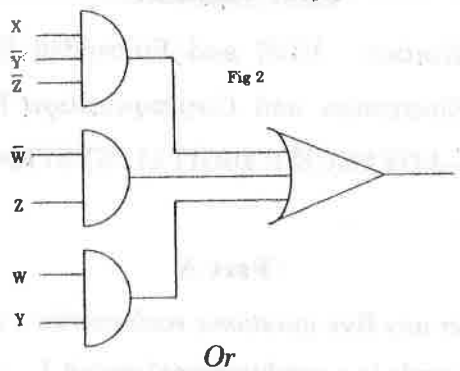


Fig 2

(20 marks)

Or

12. Design a clocked synchronous state machine with state/output table shown in Fig. 3, using D flip-flops. Use two state variables Q_1, Q_2 with the state assignment A = 00, B = 01, C = 11, D = 10.

	X		
S	0	1	Z
A	B	D	0
B	C	B	0
C	B	A	1
D	B	C	0
	S*		

(20 marks)

13. (a) Discuss the merits and demerits associated with FPGA based design. (10 marks)

(b) Give the architecture of Xilinx 4000 series logic cell and give its important features. (10 marks)

Or

14. Obtain the PLA equivalent circuit for the following, with minimum number of rows in the PLA structure :

$$z_1 = a.b + \bar{a}\cdot\bar{b}\cdot\bar{c}\cdot\bar{d}$$
$$z_2 = a\cdot\bar{c} + \bar{a}\cdot\bar{c}\cdot d + b$$
$$z_3 = a\cdot b + a\cdot\bar{c} + \bar{a}\cdot\bar{b}\cdot\bar{d}$$
$$z_4 = a\cdot c + a\cdot\bar{b}\cdot c + \bar{a}\cdot b\cdot d$$

(20 marks)

15. Design verilog program to implement a divide-by-five counter. (20 marks)

Or

16. Write the verilog program to realise a 4 bit shift right register. (20 marks)

[4 × 20 = 80 marks]

G 2956 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JULY 2010

First Semester

Specialization : VLSI and Embedded Systems

Branch : Electronics and Communication Engineering

LMV-104—INTRODUCTION TO VLSI TECHNOLOGY AND DESIGN

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions, each carries* 4 *marks.*

1. Explain various properties of oxides.
2. Describe the principle of ion implantation.
3. Write a note on projection printing in optical lithography.
4. Explain multilevel metalisation.
5. Compare *n*-well CMOS and BiMOS technologies.
6. What is self aligned polysilicon gate NMOS process ? Explain.
7. Discuss the double metal CMOS process design rules.
8. Draw the layout diagram for two input NOR gate.

(5 × 4 = 20 marks)

Part B

Answer **all** *questions, each carries* 20 *marks.*

9. Describe the growth patterns of epitaxial and oxide layers in any two types of processes, giving neat diagrams.

(20 marks)

Or

10. With the help of neat diagrams, list and explain the possible ways of growing an oxide on a substrate without forming oxidation induced stacking faults.

(20 marks)

11. List the various types of CVD techniques and with neat sketches, describe any *two* of them in detail.

(20 marks)

Or

12. Describe reactive ion etching and parallel plate plasma etching techniques. Compare their advantages and limitations.

(20 marks)

Turn over

13. (a) How the threshold voltage of MOS transistor is reduced ? Also discuss the scheme for increasing speed of MOS transistor.

(10 marks)

(b) What do you understand by stick diagram ? Explain the role of stick diagram in fabrication of MOS ICs ?

(10 marks)

Or

14. (a) What is the minimum area transistor ? How is the chip area estimated using minimum area transistor for a given IC ? Explain with any example.

(10 marks)

(b) With necessary diagrams, explain a shallow trench isolation for CMOS. (10 marks)

15. (a) What are the problems encountered due to wiring capacitance ? How they are minimized ?

(8 marks)

(b) Draw the schematic of an IC based on BiC MOS technology and describe them. (12 marks)

Or

16. (a) Draw neat sketches of simple MOS circuits. (10 marks)

(b) Describe clearly the ASIC fabrication techniques. (10 marks)

[4 × 20 = 80 marks]

G 2957 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JULY 2010

First Semester

Specialization : VLSI and Embedded System

Branch : Electronics and Communication Engineering

LMV-105-1—WIRELESS COMMUNICATION

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions, each carries* 4 *marks.*

1. Distinguish between narrow band and wide band fading models.
2. What is space diversity ? List is merits.
3. Clearly explain the vehicle locating methods in a cellular system.
4. Define Grade of service and how it can be improved.
5. What is hand off ? How it is delayed ?
6. How multipath fading is eliminated in CDMA ?
7. Define and explain fast and slow frequency hopping.
8. What are the advantages of using CDMA for a cellular network ?

(5 × 4 = 20 marks)

Part B

Answer **all** *questions, each carries* 20 *marks.*

9. Compare the average probability of bit error for BPSK under MRC versus EGC, assuming two-branch diversity with i.i.d. Rayleigh fading on each branch and average branch SNR $\overline{\gamma} = 10$ dB.

(20 marks)

Or

10. Describe the different propagation models for wireless communication networks. (20 marks)

11. (a) Assume a Rayleigh fading channel with average signal power $2\sigma^2 = -80$ dBm. What is the power outage probability of this channel relative to the threshold $P_0 = -95$ dBM ? How about $P_0 = -90$ dBm ?

(10 marks)

(b) Explain the concept of frequency reusage in cellular system. (10 marks)

Or

Turn over

12. (a) Is it possible to jam CDMA ? Explain clearly. (10 marks)

(b) To address the service to be increased in the number of MSs in a CDMA system, it was decided to use TDMA as well. Is it possible to do so ? If yes, how ; and if no, why not ? (10 marks)

13. (a) With a neat block diagram, explain the principle of two-user multicarrier CDMA system. (14 marks)

(b) Show that, for any real periodic spreading code $S_c(t)$, its autocorrelation $\rho_c(\tau)$ over one period is symmetric about τ and reaches its maximum value at $\tau = 0$. (6 marks)

Or

14. (a) Calculate the base bandwidth of one chip in a spreading case $S_c(t)$ with chip time $T_c = 1\mu S$. (6 marks)

(b) With a neat diagram, describe the working of a Rake receiver. (14 marks)

15. Clearly explain the services provided by 3G cellular system. Explain harmonized 3G systems. (20 marks)

Or

16. Describe the GSM infrastructure, indicating the different standard channels. (20 marks)

[4 × 20 = 80 marks]

G 2958 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JULY 2010

First Semester

Specialization : VLSI and Embedded System

Branch : Electronics and Communication Engineering

LMV-106-2—DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEM

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions, each carries* 4 *marks.*

1. Explain what is meant by instruction pipelining.
2. Why MAC operation is implemented in hardware in programmable DSP ?
3. Explain any two arithmetic instructions in TMS 320 C6XXX.
4. What is the use of HPI in C6X ?
5. Write the magnitude square function and frequency response of Butterworth and Chebyshev analog filters.
6. State and prove periodicity for DFT.
7. What is the function of EMIF in C6X ?
8. Explain the functions and advantages of EDMA controller.

(5 × 4 = 20 marks)

Part B

Answer **all** *questions, each carries* 20 *marks.*

9. Clearly explain the various registers in TMS 320C6XXX and mention their functions.

Or

10. With a neat diagram, explain the VLIW architecture and mention its merits.

11. (a) Describe the different ways in which the auxiliary register pointer can be updated.

    (b) Give the list of the mnemonics of shift/logical expressions of C6X and explain them clearly.

Or

12. Write a program which processes the input data from the AIC on real time basis and display the LP filtered output in the CCS output screen. Assume the LPF to have 81 taps and to be stored in the program-memory area.

13. Design a low-pass digital filter to be used in an A/D – H(z) – D/A structure that will have a – 3 dB cut-off at 30π rad./sec. and an attenuation of 50 dB at 45π rad./sec. The filter is required to have a linear phase and the system will use a sampling rate of 100 samples/sec.

Or

Turn over

14. (a) For N = 5, compute the DFT of $x_1(n) = (1, 1, 1, 0, 0)$ and compare the result with the DFT of $x_2(n) = (1, 1, 1)$ for N = 3.

(b) Find the 4 point real sequence $x(n)$ if its 4 point DFT samples are X (0) = 6, X (1) = $-z + jz$, X (2) = $-z$. Use DIF – FFT algorithm.

15. With neat internal architectural diagram, explain the functioning of a DSP controller.

Or

16. What is pipe lining ? With reference to pipeline, explain pipeline depth, interlocking and branching effects.

(4 × 20 = 80 marks)