

**M.TECH. DEGREE EXAMINATION, MARCH 2013****First Semester**

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded System

**MECVE 101—SEMICONDUCTOR DEVICES—PHYSICS AND TECHNOLOGY**

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

*Answer all the questions, each full question carries 25 marks.*

1. (a) Derive the continuity equation for an  $n$ -type semiconductor. (8 marks)
- (b) What is the electron concentration in terms of the donor impurity concentration. (5 marks)
- (c) Explain the minority carrier distribution of a PN Junction diode and its effect on junction capacitance. (12 marks)

*Or*

2. (a) Derive the intrinsic carrier concentration under thermal equilibrium condition. (12 marks)
- (b) With neat diagrams, explain the following :
- (i) Abrupt Junction. (13 marks)
- (ii) Linearly graded Junction. (13 marks)
3. (a) Derive the basic Eber Moll's equation for a PNP transistor. (12 marks)
- (b) Describe the basic operation of a Enhancement mode MOSFET. (13 marks)

*Or*

4. (a) Explain the frequency response and switching characteristics of a BJT. (12 marks)
- (b) Write brief notes on :
- (i) CCD. (13 marks)
- (ii) BiCMOS.

**Turn over**

5. (a) With neat sketch explain the thermal oxidation of silicon. (8 marks)
- (b) Describe the kinetics of Thermal oxidation of Silicon. (7 marks)
- (c) Brief about the importance of Low  $k$  constant materials in VLSI circuits. (10 marks)

Or

6. (a) Describe in detail about Implant damage and Annealing process. (12 marks)
- (b) Explain the Technique of Ion Implantation. (13 marks)
7. (a) Discuss any two next generation Lithography techniques for ULSI/VLSI. (12 marks)
- (b) Explain the ion beam sputtering technique. (13 marks)

Or

8. (a) Describe the CVD technique of Dielectric Deposition. (12 marks)
- (b) What are the major distinctions between the traditional RIE and High density plasma Etching? (13 marks)

[4 × 25 = 100 marks]

**M.TECH. DEGREE EXAMINATION, MARCH 2013**

**First Semester**

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded Systems

**MECVE 102—ADVANCED DIGITAL SYSTEM DESIGN**

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

Answer all questions.

Each full question carries 25 marks.

- I. (a) Design a synchronous sequential circuit to meet the following specifications. The circuit has one input  $w$  and one output  $z$ . All changes in the circuit occurs on positive edge of clock signal. The output  $z$  is equal of 1, if during two immediately preceding clock cycles the input " $w$ " was equal to 1. Otherwise, the value of  $z$  is equal to 0. Use D-flip-flops to design the circuit.

(20 marks)

- (b) Differentiate between Moore type and Mealy Type machines.

(5 marks)

Or

- II. (a) Design synchronous counter using J-K flip-flop to count in the following random sequence 0, 3, 1, 4, 2, 7, 0, 3, 1, 4, 2, 7, ....

(18 marks)

- (b) Minimize the following state Table.

Present State	Next state		Output $z$
	$w = 0$	$w = 1$	
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

(7 marks)

**Turn over**

III. (a) The minimum cost function of a circuit is :

$$Y_m = CD + \bar{C} y_m$$

$$Y_s = \bar{C} y_m + C y_s$$

The minimum cost implementation results in static hazard. Design Hazard free circuit.

(10 marks)

(b) Design an asynchronous circuit that meet the following specifications. The circuit has two inputs :  $x_1$  and  $x_2$  and a single output  $z$ . The input  $x_1$  and  $x_2$  never change or are 1 simultaneously. The output  $z = 1$  is to occur only during the input state  $x_1 x_2 = 01$  and then if and only if the input state  $x_1 x_2 = 01$  is preceded by the input sequence  $x_1 x_2 = 01, 00, 10, 00, 10, 00$ .

(15 marks)

Or

IV. Explain the following using suitable example. (i) Primitive flow table. (ii) Flow Table. (iii) State assignment. (iv) Dynamic hazard. (v) One hot state assignment.

(5 × 5 = 25 marks)

V. (a) State the difference between PLA and PAL.

(5 marks)

(b) Draw the schematic of the configurable logic block of Xilinx FPGA and explain.

(13 marks)

(c) Explain how logic function can be implemented using EPROM.

(7 marks)

Or

VI. (a) Discuss about (i) Gate array logic. (ii) EPLD.

(12 marks)

(b) Draw the cross-section of FAMOS (Floating gate Avalanche metaloxide semiconductor) device used as cell in EPROM and explain its function.

(13 marks)

VII. (a) Explain the following : (i) user defined primitives. (ii) operators in verilog HDL.

(10 marks)

(b) Write the verilog code for D-type flip-flop (i) with synchronous control ; (ii) with asynchronous control.

(15 marks)

Or

VIII. (a) Write the verilog code for 4 bit binary up-down counter and explain.

(15 marks)

(b) Name the different types of modelling in VHDL and explain about each one.

(10 marks)

[4 × 25 = 100 marks]

**M.TECH. DEGREE EXAMINATION, MARCH 2013****First Semester**

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded System

MECVE 103—CMOS VLSI DESIGN

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

*Answer all questions.**Each full question carries 25 marks.*

1. (a) Draw a cross-sectional view of nMOS transistor and explain its modes of operation. (15 marks)
- (b) Consider the nMOS transistor in a  $0.6 \mu\text{m}$  process with gate oxide thickness of  $100 \text{ \AA}$ . The doping level is  $N_A = 2.10^{17} \text{ cm}^{-3}$  and the nominal threshold voltage is  $0.7 \text{ V}$ . The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at  $4 \text{ V}$  instead of  $0$ ? (10 marks)

*Or*

2. (a) Design a pseudo-NMOS inverter and compare with CMOS inverter. (10 marks)
- (b) Design a  $4 : 1$  multiplexer using  $2 : 1$  multiplexers. Use CMOS transmission gates. (8 marks)
- (c) Design a 2 input XOR gate using DPTL logic and explain its operation. (7 marks)
3. (a) Compare the characteristics of Static and dynamic CMOS logic circuits with suitable example. (12 marks)
- (b) What is the use of keeper in dynamic logic circuits. (5 marks)
- (c) Explain about N-P dynamic logic circuits and list out its advantages. (8 marks)

*Or*

4. (a) Explain in detail the noise problem in dynamic logic circuits. How it is rectified? (13 marks)
- (b) What is race problem? How it is rectified in NORA logic? Explain. (12 marks)
5. (a) What are the advantages and disadvantages of Bi-CMOS logic circuits? Draw a standard Bi-CMOS structure of inverter and explain. (13 marks)
- (b) Explain about SOI CMOS static logic circuits. (12 marks)

*Or*

Turn over

6. (a) Design a 2 input NAND gate using sub-3V BiCMOS structure. Explain its operation. (13 marks)
- (b) Draw and explain a 1.5 V Bi-CMOS dynamic logic circuits. (12 marks)
7. (a) Explain the two different types of scaling laws used in sub micron technologies. (10 marks)
- (b) Explain the design issues and solutions for deep sub-micron sub-system design. (15 marks)

Or

8. (a) Write the applications of high speed multipliers. Explain any one of the high speed multiplier. (15 marks)
- (b) Explain in detail symbolic layout system. (10 marks)

[4 × 25 = 100 marks]

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**M.TECH. DEGREE EXAMINATION, MARCH 2013**

**First Semester**

**Branch : Electronics and Communication Engineering**

**Specialization : VLSI and Embedded System**

**MEC VE 104—EMBEDDED SYSTEM DESIGN**

**(Regular/Supplementary)**

Time : Three Hours

Maximum : 100 Marks

*Answer all questions.*

*Each full question carries 25 marks.*

I. (a) With the help of diagram explain how a desired functionality can be implemented using :

(i) Application specific processor.

(ii) Single purpose processor.

(15 marks)

(b) Explain the ideal top-down design process.

(10 marks)

*Or*

II. (a) Discuss about the following :

(i) Time to market Design metric.

(ii) NRE and unit cost Design metrics.

(14 marks)

(b) Distinguish between Full Custom IC technology and semi custom IC technology.

(11 marks)

III. (a) Explain how data path can be constructed using four step process with an example.

(15 marks)

(b) Design a instruction set simulator for a simple processor with the following instructions  
MoV R<sub>n</sub>, direct ; MoV direct R<sub>n</sub> ; MoV@ R<sub>n</sub>, R<sub>m</sub> ; MoV R<sub>n</sub>, # imm ; ADD R<sub>n</sub>, R<sub>m</sub> ; SUB R<sub>n</sub>, R<sub>m</sub>.

(10 marks)

*Or*

IV. (a) Explain the testing and de-bugging phases of developing programs for an application.

(13 marks)

(b) List the major varieties of Application specific Instruction set processors (ASIPs) and explain about each one.

(12 marks)

**Turn over**

V. (a) What for a watchdog timer is used in an embedded application ? Explain its function. Also explain how watchdog Timer can be used in ATM Time out ?

(10 marks)

(b) Draw the pulse width modulator (PWM) circuit in block diagram form and explain its operation. Also explain how p.w.m. circuit can be used to control the speed of a DC motor.

(15 marks)

Or

VI. (a) Draw the schematic of  $4 \times 4$  matrix keyboard and explain how the keyboard controller dated a key press and generate the corresponding hex Code of the activated key.

(15 marks)

(b) Discuss about I<sup>2</sup>C serial protocol.

(10 marks)

VII. (a) Draw the basic DRAM architecture and explain.

(10 marks)

(b) What is meant by functional and non-functional requirement of specifications ? Explain about the high level functionality of digital camera using flowchart.

(15 marks)

Or

VIII. (a) Explain the following :

(i) Fast page Mode DRAM (FPM, DRAM).

(ii) Memory hierarchy and Cache.

(iii) NVRAM (NM volatile RAM).

(15 marks)

(b) Explain the function of UART and CCDPP (Charge Coupled Device pre-processing) used in digital camera with the help of FSM (finite state machine with data).

(10 marks)

[4 × 25 = 100 marks]



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**M.TECH. DEGREE EXAMINATION, MARCH 2013**

**First Semester**

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MECVE 105.1—ASIC DESIGN (Elective I)

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

*Answer all questions.*

*Each full question carries 25 marks.*

1. Compare and explain the features of standard cell based Asics and gate array based Asics with their structures. (25 marks)

*Or*

2. (a) Explain : (15 marks)  
(i) PLDs and (ii) FPGAs.  
(b) Explain in detail the ASIC design flows. (10 marks)

3. (a) Explain the following technologies : (15 marks)  
(i) Static RAM. (ii) EPROM.  
(iii) EEPROM.

- (b) Explain with example the wheel structure of ACTI logic module. (10 marks)

*Or*

4. (a) Implement the Boolean function  $F = \bar{A}B + \bar{C}D + \bar{B}\bar{C} + AC\bar{D}$  using logic expanders and programmable inversion in Altra MAX FPGA that contains a registered PAL with 4 inputs, 3 product terms and 10 macro cells. Compare these two implementations. (15 marks)  
(b) Explain about PREP bench marks. (10 marks)

5. Explain in detail how to realize a sequential circuit using programmable logic devices. (25 marks)

*Or*

6. Explain the different types of state machines and realize any one of the state machine using Xilinx FPGA. (25 marks)

**Turn over**

- 7. (a) Explain about verilog operators. (15 marks)
- (b) Design a 4 : 1 multiplexer using 2 : 1 multiplexer. Write its verilog code. (10 marks)

Or

- 8. (a) Explain about the Compilation and Simulation of Verilog Codes. (10 marks)
- (b) Design a 4 bit serial adder using structural modelling of Verilog HDL. (15 marks)

[4 × 25 = 100 marks]

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**M.TECH. DEGREE EXAMINATION, MARCH 2013**

**First Semester**

Branch—Electronics and Communication Engineering

Specialization : VLSI and Embedded System

**MECVE 106-1—PROCESSOR ARCHITECTURE AND PARALLEL PROCESSING**  
(Elective-II)

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

*Answer all questions.*

*Each full question carries 25 marks.*

- I. (a) Explain how pipeline helps to increase the through put of a processor. ( 10 marks)  
(b) Draw the SPARC-II internal architecture in block diagram form and explain. (15 marks)

*Or*

- II. (a) Discuss about the SPARC pipeline and also explain how it avoids the hazard. (15 marks)  
(b) List and explain the advantages and disadvantages of RISC processor. (10 marks)
- III. (a) Discuss about (i) large grain data flow ; (ii) RISC data flow. (20 marks)  
(b) What are data flow processors ? (5 marks)

*Or*

- IV. (a) Explain in-order execution and out-of-order execution with examples. (15 marks)  
(b) Compare data flow with control flow. (10 marks)
- V. (a) Explain the dynamic branch prediction mechanism. (15 marks)  
(b) Discuss about the principles of VLIW processors. (10 marks)

*Or*

- VI. Explain how multiple instruction issue can be achieved using dynamic scheduling. Explain the algorithm involved. (25 marks)

**Turn over**

VII. (a) Explain what is meant by coarse-grain parallelism ? Also compare fine grain and coarse grain parallelisms.

(15 marks)

(b) List the benefits of processor in memory and explain how they are achieved ? (10 marks)

*Or*

VIII. (a) Explain the concept of re-configurable computing. (15 marks)

(b) Explain how multi threading approach can be used for tolerating latencies. (10 marks)

[4 × 25 = 100 marks]