G 486 (Pages : 2) Reg. No....ECE M.Tech

Name.....

M.TECH. DEGREE EXAMINATION, MARCH 2012

First Semester

Branch—Electronics and Communication Engineering

Specialization—VLSI and Embedded System

LMV 102—CMOS DIGITAL INTEGRATED CIRCUITS

(Supplementary—Prior to 2011 Admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions.*
Each question carries 4 *marks.*

1. Explain about different regions of MOS transistors.
2. What is Latch up ? How it is prevented ?
3. Consider a 2 input NAND gate with transistor widths chosen to achieve unit resistance, assuming PMOS have twice the resistance of NMOS transistor. Find out its logical effort and parasitic delays.
4. Explain about time borrowing concept in clocking schemes.
5. A 90 nm long transistor has a gate oxide thickness of 16 Å. What is its gate capacitance per micron of width ?
6. Design a edge triggered D-Flip-flop using transmission gates.
7. Design a 2 : 4 decoder using CMOS logic gates.
8. Explain the working principle of Barrel shifter.

(5 × 4 = 20 marks)

Part B

Answer any **four** *questions.*
Each question carries 20 *marks.*

9. Explain in detail all the second order effects of MOS transistor. (20 marks)

Or

10. (a) With neat diagrams, explain the CMOS fabrication process. (14 marks)

    (b) What is stick diagram ? Draw a stick diagram of CMOS invertor. (6 marks)

Turn over

11. (a) Find the rising and falling propagation delays of an AND-OR INVERT gate using the Elmore delay model. Estimate the diffusion capacitance based on a stick diagram of the layout. (14 marks)

(b) Write short notes about pulsed latches. (6 marks)

Or

12. (a) Compare the static and dynamic CMOS invertors. (6 marks)

(b) Explain the read/write operation of the SRAM cell. (14 marks)

13. Explain in detail DC and Transient characteristics of CMOS invertor. (20 marks)

Or

14. (a) Explain with example, how the CMOS invertor drive the large capacitance loads. (10 marks)

(b) Write short notes about ratioed invertors. (10 marks)

15. (a) Design a carry look ahead adder and explain its operation. (12 marks)

(b) Write about high speed adders. (8 marks)

Or

16. Explain in detail the following multipliers :

(a) Array multiplier. (10 marks)

(b) Serial multiplier. (10 marks)

[4 × 20 = 80 marks]

G 487 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, MARCH 2012

First Semester

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded System

LMV 103—ADVANCED DIGITAL SYSTEM DESIGN

(Supplementary—Prior to 2011 admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions.*
Each question carries 4 *marks.*

1. Name the causes for a fault in a circuit.
2. What is a strongly connected sequential network ?
3. Draw the excitation table for JK flip-flop.
4. What is a static hazard ?
5. State the difference between PLA and PAL.
6. What is a macro cell ?
7. Write the verilog code to create a D-latch.
8. Name the different types of modeling of verilog HQL.

(5 × 4 = 20 marks)

Part B

Answer any **four** *questions.*
Each question carries 20 *marks.*

9. Design a synchronous sequential circuit to meet the following specifications. The circuit has one input w and one output z. All changes in the circuit occurs on positive edge of clock signal. The output $z = 1$ of during two immediately preceding clock cycles the input w was equal to 1. Otherwise, the value of z is equal to 0. Use D flip-flops to design the circuit.

Or

10. Draw the circuit representation for the expression :

$$F = \left(\overline{(\bar{x}_2\bar{x}_3 + x_2x_3) + x_1}\right)$$

Using the Boolean difference method determine the tests for checking all single node stock at faults.

Turn over

11. Design an asynchronous circuit to meet the following specifications. The circuit has two inputs x_1 and x_2 and a single output z. The input x_1 and x_2 never change or are 1 simultaneously. The output $z = 1$ is to occurr only during the input state $x_1x_2 = 01$ and then if and only if the input state $x_1x_2 = 01$ is preceded by the input sequence $x_1x_2 = 01, 00, 10, 00, 10, 00$.

Or

12. Explain the following using suitable example :—

    (i) Primitive flow table. (ii) Flow table.

    (iii) State arrangement. (iv) Dynamic hazard.

13. Draw the schematic of the configurable logic block of Xlinx FPGA and explain.

Or

14. Discuss about (i) CPLD ; (ii) Macrocell in a PAL device.

15. Explain the algorithm used for binary division and also write the verilog code for the same.

Or

16. Design a 16 : 1 multiplexes using two 8 : 1 multiplexers and write the verilog code for the same.

(4 × 20 = 80 marks)

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Name.....

M.TECH. DEGREE EXAMINATION, MARCH 2012

First Semester

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded System

LMV 104—INTRODUCTION TO VLSI TECHNOLOGY AND DESIGN

(Supplementary—Prior to 2011 Admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions.*
Each question carries 4 *marks.*

1. Describe the plasma enhanced CVD.
2. Discuss briefly about reactive Ion beam Etching.
3. Give a valid argument over, why the interconnects are made of Low K constant materials.
4. What is the role of negative photoresist in IC fabrication ? Explain.
5. Explain the techniques to prevent latch up.
6. Why NMOs technology is preferred over PMOs technology ?
7. Illustrate the essential characteristics of an FPGA.
8. Write a short note on structural Gate Array.

(5 × 4 = 20 marks)

Part B

Answer **all** *the questions.*
Each question carries 20 *marks.*

9. (a) Discuss in detail about the kinetics of SiO_2 growth for both thick and thin films. (12 marks)

(b) Describe the impact of lateral diffusion and impurity redistribution on device characteristics. (8 marks)

Or

10. (a) Describe the wet chemical etching method for Si and SiO_2 in semiconductor processing. (8 marks)

(b) Discuss in detail about the ion implantation damage and Annealing. (12 marks)

Turn over

11. (a) Explain the E beam lithography and discuss about the proximity effect. (12 marks)

(b) Discuss in detail about the Aluminium metallization and its relative problems. (8 marks)

Or

12. (a) With neat diagrams explain the optical lithography. (12 marks)

(b) With neat diagrams explain the following :—

(i) PECVD.

(ii) LPCVD. (8 marks)

13. (a) Explain the SOI process in detail. (12 marks)

(b) Describe the fabrication process for the following circuit elements :—

(i) Capacitors.

(ii) Resistors. (8 marks)

Or

14. (a) With neat diagrams explain the nwell process and discuss its relative merits and demerits. (12 marks)

(b) Write short note on :

(i) PLDs.

(ii) FPGA. (8 marks)

15. (a) With neat sketch explain standard cell based ASICs. (12 marks)

(b) Explain the λ based design rules and draw the layout of 3 i/p NAND gate and estimate its area. (8 marks)

Or

16. (a) Explain the ASIC design flow chart. (8 marks)

(b) What are the different types of Gate Array-based ASICs ? Explain them briefly. (12 marks)

[4 × 20 = 80 marks]

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Name.....

M.TECH. DEGREE EXAMINATION, MARCH 2012

First Semester

Branch—Electronics and Communication Engineering

Specialization : VLSI and Embedded System

LMV 105-1—WIRELESS COMMUNICATION (Elective I)

(Supplementary—Prior to 2011 Admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions.*
Each question carries 4 *marks.*

1. Consider an indoor wireless LAN with f_c = 900 MHz, cells of radius 100 m, and nondirectional antennas. Under free space path loss model, what transmit power is required at the access point in order for all terminals within the cell to receive a minimum power of 10 μW.
2. What is meant by equal gain combining ? Explain.
3. Write the concepts of FDM and TDM.
4. Explain how cochannel interference effect is reduced in cellular system.
5. Write the properties of maximal length sequences used in CDMA systems.
6. Draw the RAKE receiver and explain.
7. Explain the signal processing in GSM.
8. Give the capacity of MIMO channels.

(5 × 4 = 20 marks)

Part B

Answer **all** *questions.*
Each question carries 20 *marks.*

9. (a) Find the outage probability of BPSK modulation at $P_b = 10^{-3}$ for a Rayleigh fading channel with selection combining diversity for M = 1 (no diversity), M = 2 and M = 3. Assume equal branch SNRs of $\bar{r}$ = 15 dB (average). (8 marks)

(b) Explain the concept of Maximal ratio combining with neat diagram. (12 marks)

Or

Turn over

10. (a) Derive the impulse response model of a multipath channel. (10 marks)

(b) Discuss the performance of digital modulation schemes over wireless channels. (10 marks)

11. (a) A receiver in an Urban cellular system detects a 1 mW signal at $d = d_0 = 1$ m. from a transmitter. In order to mitigate cochannel interference effects, it is required that the signal received at any base station receiver from another base station transmitter which operates with the same channel must be below –110 dBm. Path loss exponent is 3. Determine the major radius of each cell if a 7 cell reuse pattern is used.

(10 marks)

(b) Discuss the blocked calls cleared and blocked calls delayed systems. (10 marks)

Or

12. (a) Explain the handoff strategies used in cellular system and discuss the practical problems in handoff.

(10 marks)

(b) Explain the channel assignment strategies used in cellular system. (10 marks)

13. (a) Write the difference between hard handoff and soft handoff. (10 marks)

(b) Discuss the capacity of CDMA networks. (10 marks)

Or

14 Discuss the concepts of direct sequence and frequency hopping spread spectrum systems with example.

(20 marks)

15. (a) If GSM uses a frame structure where each frame consists of 8 time slots, and each time slot contains 156.25 bits, and data is transmitted at 270.833 kbps in the channel. Find the time durations of a bit, slot and a frame.

(5 marks)

(b) Discuss the capacity of flat and frequency selective fading channels. (15 marks)

Or

16. (a) Draw the block diagrams of IS-95 forward and reverse channel modulation process for a single user and explain.

(15 marks)

(b) Consider a MIMO channel with gain matrix $H = \begin{bmatrix} .7 & .9 & .8 \\ .3 & .8 & .2 \\ .1 & .3 & .9 \end{bmatrix}$.

Find the capacity of this channel under beam forming, given the channel knowledge at the transmitter and receiver, B = 100 kHz and P = 10 dB.

(5 marks)

[4 × 20 = 80 marks]

G 491 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, MARCH 2012

First Semester

Branch : Electronics and Communication Engineering

Specialization—VLSI and Embedded System

LMV 106.2—DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS (Elective II)

(Supplementary—Prior to 2011 admissions)

Time : Three Hours Maximum : 100 Marks

Part A

Answer any **five** *questions.*
Each question carries 4 *marks.*

1. List the key features of TMS 320C6X processor.
2. Explain the on-chip program/Data cache memory operation of TMS 320C6X processor.
3. What are the instructions .L functional unit support in TMS3 20C6X ?
4. Explain the steps for code generation in Code composer studio.
5. Explain about symmetric and antisymmetric FIR filters.
6. What is the relation between DFT4 z-transform.
7. Compare the differences in the architecture of DSP and DSP controllers.
8. List the difference applications the DSPS can be used.

(5 × 4 = 20 marks)

Part B

Answer **All** *questions.*
Each question carries 20 *marks.*

9. Draw the TMS320C62X CPU datapath diagram and explain the operation of various functional units.

Or

10. Draw the block diagram of TMS320C6X timer. Explain its modes of operation and programming steps.

11. Explain the addressing modes of TMS320C6X processor.

Or

12. Explain the code composer studio code execution steps and the debug options.

Turn over

13. Explain the basic IIR filter structures.

Or

14. Discuss the steps in the implementation of 8-point DFT using radix-2 decimation in frequency algorithm in MATLAB.

15. Explain the architecture of any DSP controller and its applications.

Or

16. Explain any *one* application that can be implemented in DSPs.

(4 × 20 = 80 marks)