G 1128

Reg. No.....

Name.....

# M.TECH. DEGREE EXAMINATION, APRIL/MAY 2014

**First Semester**

Branch : Electronics and Communication Engineering

Specialisation : VLSI and Embedded Systems

MECVE 102—CMOS ANALOG 1C—I

(Regular—2013 Admissions)

Time : Three Hours

Maximum : 100 Marks

*Answer* **all** *questions.*
*Each question carries* 25 *marks.*

1. (a) Draw cascade current mirror and derive sensitivity expression for a CMOS current mirror.

   (b) Explain with example: Current source self-biasing.

(12 + 13 = 25 marks)

*Or*

2. (a) Design a 2.5 V reference using MOSFET only voltage divider assuming $V_{DD}$ = +5 V and $V_{ss}$ = 0V. Also determine the temperature coefficient of reference.

   (b) Explain advanced voltage references in brief.

3. (a) Explain the concept of noise bandwidth for a differential amplifier.

   (b) Explain wide wing differential amplifiers.

(12 + 13 = 25 marks)

*Or*

4. (a) Explain current differential amplifier.

   (b) Explain CMOS Class AB output stage.

5. (a) Explain source cross couple pair.

   (b) What is the significance of CMRR of differential amplifier ?

(12 + 13 = 25 marks)

*Or*

6. (a) Explain differential amplifier with source follower as an output stage.

   (b) Compare basic configurations of single stage amplifiers.

7. (a) What are the types of noise? Which one is significant most ? Why ?

   (b) State the types of noise. Explain how noise is represented in circuits.

(12 + 13 = 25 marks)

*Or*

8. (a) Explain thermal noise and noise in differential pairs.

   (b) Explain the effect of noise in Common Gate stage.

[4 × 25 = 100 marks]

G 1150 (Pages : 2) Reg. No.....

Name.....

# M.TECH. DEGREE EXAMINATION, APRIL/MAY 2014

**First Semester**

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded Systems

MECVE 103 – CMOS DIGITAL DESIGN – I

(Regular – 2013 Admissions)

Time : Three Hours Maximum : 100 Marks

*Answer* **all** *questions.*
*Each full question carries* 25 *marks.*

1. (a) Explain delay in multistage logic networks.

   (b) Write down the limitations of logical effort.

   (15 + 10 = 25 marks)

*Or*

2. (a) Explain pass transistor DC characteristics in detail.

   (b) Explain in detail about delay models.

   (10 + 15 = 25 marks)

3. (a) Explain in detail about low swing signaling.

   (b) Discuss the logical effort with wires.

   (15 + 10 = 25 marks)

*Or*

4. (a) Explain cross talk and what are the techniques used to control the cross talk in interconnect wires.

   (b) Explain on various interconnect parasitic effects in detail.

   (15 + 10 = 25 marks)

5. (a) Explain multi output Domino logic in detail.

   (b) Write down the advantages and disadvantages of SOI.

   (15 + 10 = 25 marks)

*Or*

6. Explain in detail : (a) NORA ; (b) TSPC.

   (25 marks)

**Turn over**

7. (a) How Kernighan-Lin algorithm can be used for partitioning? Explain with a suitable example.

   (b) Explain full custom flow with the help of design flow chart.

(15 + 10 = 25 marks)

*Or*

8. (a) Explain global routing and detailed routing with an example.

   (b) Explain design for testability in detail.

(15 + 10 = 25 marks)

[4 × 25 = 100 marks]

G 1173 (Pages : 2) Reg. No.....

Name.....

# M.TECH. DEGREE EXAMINATION, APRIL/MAY 2014

**First Semester**

Branch : Electronics and Communication

Specialization : VLSI and Embedded Systems

MECVE 104 – EMBEDDED SYSTEM HARDWARE ARCHITECTURE – I

(Regular – 2013 Admissions)

Time : Three Hours Maximum : 100 Marks

*Answer* **all** *questions.*
*Each question carries* 25 *marks.*

1. (a) Classify MCU's in detail.
   (b) Compare microprocessor and microcontroller.
   (c) Write a short note on brain machine interface.

(10 + 10 + 5 = 25 marks)

*Or*

2. Explain embedded system architecture in detail. Give an example for embedded systems and explain in detail.

(25 marks)

3. (a) Explain ISA architecture models.
   (b) Discuss the SSEM.

(15 + 10 = 25 marks)

*Or*

4. Write a short notes on :
   (a) Processor performance bench marks.
   (b) Importance of reading a schematic.

(25 marks)

5. Explain an embedded board memory in detail.

(25 marks)

*Or*

6. (a) Discuss the direct memory access.
   (b) Explain the memory spaces.

(15 + 10 = 25 marks)

**Turn over**

7. (a) Explain bus arbitration and timing.

   (b) Explain the bus performance.

(15 + 10 = 25 marks)

*Or*

8. (a) Explain in detail about IEEE 802.111 wireless LAN serial 110 standard.

   (b) Explain in detail about 12C bus with the help of required timing diagrams.

(15 + 10 = 25 marks)

[4 × 25 = 100 marks]

G 1201 (Pages : 2) Reg. No.....

Name.....

# M.TECH. DEGREE EXAMINATION, APRIL/MAY 2014

**First Semester**

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded Systems

MECVE 105-2 – VLSI PROCESS TECHNOLOGY

(Regular – 2013 Admissions)

Time : Three Hours Maximum : 100 Marks

*Answer* **all** *questions.*
*Each full question carries* 25 *marks.*

1. (a) Explain in detail about the hot processing and state the microscopic models.
   (b) Briefly explain the semiconductor substrates for IC fabrication.

(12 + 13 = 25 marks)

*Or*

2. (a) Explain the need of thin film grown techniques and its types.
   (b) Explain the Fick's second law of diffusion.

(12 + 13 = 25 marks)

3. (a) Explain the working principle of MOCVD.
   (b) Explain the importance of implantation modelling.

(12 + 13 = 25 marks)

*Or*

4. (a) Briefly explain the working mechanism of PECVD.
   (b) Explain the working mechanism and applications of MBE.

(12 + 13 = 25 marks)

5. (a) Discuss in detail about the non-optical lithography.
   (b) Briefly explain the photoresists and state the polymeric material properties.

(12 + 13 = 25 marks)

*Or*

6. (a) Describe in detail about the advanced lithographic techniques.
   (b) Discuss the chemical polishing technology.

(12 + 13 = 25 marks)

**Turn over**

7. (a) State the applications of the VLSI interconnect.

   (b) Explain the importance of MEMS technology.

(15 + 10 = 25 marks)

*Or*

8. (a) State the different stages of fabrication of MEMS.

   (b) Write in detail about the device Isolation.

(15 + 10 = 25 marks)

[4 × 25 = 100 marks]

**G 1243** (Pages : 2) Reg. No.....

Name.....

# M.TECH. DEGREE EXAMINATION, APRIL/MAY 2014

**First Semester**

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded Systems

MECVE 106-1 – VLSI CAD

(Regular – 2013 Admissions)

Time : Three Hours Maximum : 100 Marks

*Answer* **all** *questions.*
*Each full question carries* 25 *marks.*

1. (a) Explain in detail about the physical design automation.
   (b) State the Bellmann-Ford algorithm.

(12 + 13 = 25 marks)

*Or*

2. (a) Explain the steps involved different graph algorithms.
   (b) Explain the design rules present in the case of physical design.

(12 + 13 = 25 marks)

3. (a) Explain the constructive placement and iterative improvement.
   (b) Explain the classification of partitioning algorithms.

(12 + 13 = 25 marks)

*Or*

4. (a) Briefly explain the classification of partitioning algorithms.
   (b) Explain the algorithmic steps present in simulated annealing using an example.

(12 + 13 = 25 marks)

5. (a) Discuss in detail about the optimal channel pin assignment algorithm.
   (b) Explain the concept and terminology and floor plan representation.

(12 + 13 = 25 marks)

*Or*

6. (a) Describe the problems in floor planning.
   (b) Describe in detail the integer programming based floor planning.

(12 + 13 = 25 marks)

**Turn over**

7. (a) State the channel routing algorithms.

   (b) Explain the left edge algorithm.

(15 + 10 = 25 marks)

*Or*

8. (a) State the global routing and its applications.

   (b) Write in detail about the maze's algorithm.

(15 + 10 = 25 marks)

[4 × 25 = 100 marks]