F 6914 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JANUARY 2015

First Semester

Branch : Electronics and Communication Engineering

Specialisation—VLSI and Embedded Systems

MECVE 101—SEMICONDUCTOR DEVICES–PHYSICS AND MODELLING

(New Scheme—2013 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*
Each full question carries 25 *marks.*

1. (a) Define MOS transistor. Explain the structure and operation of MOS transistor in detail. (15 marks)

   (b) What is meant by inversion ? Explain the various types of inversions. (10 marks)

Or

2. Write short notes on :

   (i) MOS capacitor ;

   (ii) Flat band voltage ;

   (iii) Potential balance and charge balance ;

   (iv) Flat band condition.

   (25 marks)

3. (a) Compare body referenced and source referenced modelling. (10 marks)

   (b) Discuss the effects of extrinsic source and drain series resistances in detail. (15 marks)

Or

4. Explain regions of inversion of the three terminal MOS structure in detail. (25 marks)

5. (a) Write down the limitations of the quasi-static model. (10 marks)

   (b) Derive the continuity equation and explain the analysis of non-quasi-static modelling. (15 marks)

Or

6. Explain in detail

(a) Carrier velocity saturation ; (b) Channel length modulation ;

(c) Hot carrier effects ; (d) Impact ionization.

(25 marks)

7. (a) Explain the following in detail :—

(a) BSIM ;

(b) EKV ;

(c) PSP.

(15 marks)

(b) Explain white noise and flicker noise in detail. (10 marks)

Or

8. (a) Compare the small signal capacitances at weak inversion, strong inversion (linear and saturation).

(15 marks)

(b) Categories MOSFET simulation models. (10 marks)

[4 × 25 = 100 marks]

F 6959 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JANUARY 2015

First Semester

Branch : Electronics and Communication Engineering

Specialisation—VLSI and Embedded Systems

MECVE 103—CMOS DIGITAL DESIGN I

(New Scheme—2013 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*
Each full question carries 25 *marks.*

1. (a) Explain gate diffusion capacitance in detail. (15 marks)

   (b) Discuss the transient response and Elmore delay. (10 marks)

Or

2. (a) With a suitable example discuss how the logical effort can be effectively used to estimate the multistage delay of a logical network. (15 marks)

   (b) Design and explain an inverter using :

   (i) NMOS ;

   (ii) CMOS ;

   (iii) Pseudo NMOS. (10 marks)

3. Explain cross talk control in detail. (25 marks)

Or

4. (a) Write a short note on :

   (i) Inductive effects ;

   (ii) Skin effect ;

   (iii) Elmore delay. (15 marks)

   (b) Write a short note on inductive voltage fluctuation along the power lines ? How this effect can be minimized in submicron technology. (10 marks)

Turn over

5. (a) Discuss and derive the floating body voltage. (10 marks)

(b) Explain the structure of SOI inverter-Write down its advantages. (15 marks)

Or

6. Explain in detail :

(i) Dual-rail Domino logic ;

(ii) Power dissipation in CMOS circuits.

(25 marks)

7. (a) Explain design for manufacturability. (10 marks)

(b) Explain in detail about :

(i) Regularity

(ii) Modularity ;

(iii) Software radio.

(15 marks)

Or

8. (a) How Kernighan-Lin algorithm can be used for partitioning ? Explain with a suitable example. (15 marks)

(b) Compare full custom and semi-custom. (10 marks)

[4 × 25 = 100 marks]

F 6983

Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JANUARY 2015

First Semester

Branch : Electronics and Communication

Specialization : VLSI and Embedded Systems

MECVE 104—EMBEDDED SYSTEM HARDWARE ARCHITECTURE—I

(New Scheme—2013 Admission onwards)

[Regular / Improvement / Supplementary]

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions. Each full question carries* 25 *marks.*

1. (a) List the hardware units that must be present in the embedded systems. (15 marks)

   (b) Explain the Exemplary applications of each type of embedded system. (10 marks)

Or

2. (a) Explain the major components of an embedded board in detail. (15 marks)

   (b) Discuss the internal processor. (10 marks)

3. (a) Draw and explain the von Neumann model. (15 marks)

   (b) Discuss the powering the hardware. (10 marks)

Or

4. Explain embedded processor in detail. (25 marks)

5. Explain memory systems in detail. (25 marks)

Or

6. (a) Discuss the memory management of external memory. (15 marks)

   (b) Explain the board of memory and interface. (10 marks)

7. (a) What is PIF, DIF and SIF time intervals and how they are used in IEEE 802.11 ? (15 marks)

   (b) Discuss in detail about SPI. (10 marks)

Or

8. (a) Compare serial and parallel I/O. (10 marks)

   (b) Explain the board buses in detail. (15 marks)

[4 × 25 = 100 marks]

F 7057 (Pages : 2) Reg. No.....

Name.....

M.TECH. DEGREE EXAMINATION, JANUARY 2015

First Semester

Branch : Electronics and Communication Engineering

Specialization : VLSI and Embedded Systems

MECVE 106—1 VLSI CAD

(New Scheme—2013 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*
Each full question carries 25 *marks.*

1. (a) Explain in detail about the VLSI design cycle.

   (b) Briefly explain the problem formulation.

   (12 + 13 = 25 marks)

Or

2. (a) Explain the applications of compaction.

   (b) Explain the longest path algorithm for DAGs.

   (12 + 13 = 25 marks)

3. (a) Explain the types of placement problem.

   (b) Explain in detail about the placement algorithms.

   (12 + 13 = 25 marks)

Or

4. (a) Briefly explain the Kerlinghan-Lin partioning algorithm.

   (b) Explain the circuit representation and wire length estimation.

   (12 + 13 = 25 marks)

5. (a) Discuss in detail about the floor planning algorithms.

   (b) Briefly explain the Hierarchical partitioning.

   (12 + 13 = 25 marks)

Or

6. (a) Describe the dead soaces in detail.

(b) Discuss the slicing and non-slicing and state the applications.

(12 + 13 = 25 marks)

7. (a) State the types of local routing problems.

(b) Explain the significance of area routing.

(15 +10 = 25 marks)

Or

8. (a) State the importance of routing and its merits and issues..

(b) Write in detail about the taxonomy on VLSI routers.

(15 + 10 = 25 marks)

[4 × 25 = 100 marks]