B

APJ Abdul Kalam Technological University

Ernakulam II Cluster

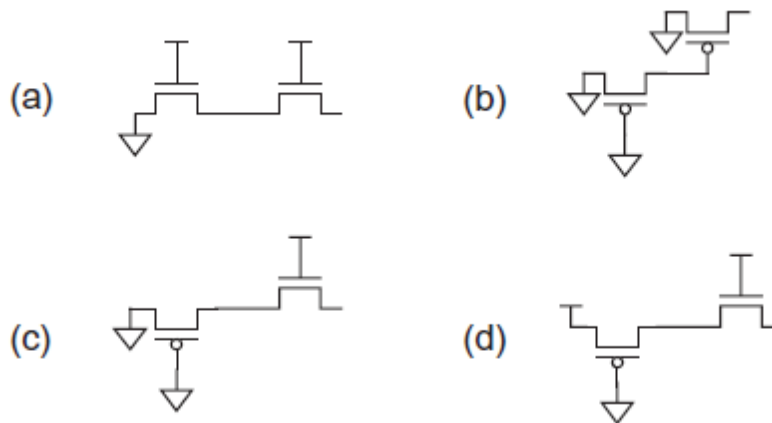**First Semester M.Tech Degree Examination December 2017**

Time : 3 hrs.   05EC 6003-CMOS DIGITAL DESIGN   Max. Marks:60

1.

a) Give an expression for the output voltage Vout for the pass transistor networks shown. Neglect the body effect. Use power supply as VDD and threshold as Vtn and Vtp.

(4 Marks)

b) Design a 3 input AND gate with equal rise and fall resistance. Model the circuit using RC network. Find the worst-case Elmore parasitic delay of 3 input AND gate.

(8 Marks)

2.

a) What is crosstalk in interconnect used in ICs. How can we eliminate cross talk.

(4 Marks)

b) Consider a 3 mm-long, 100nm wide wire. The sheet resistance is 0.08 $\Omega/\square$ and the capacitance is 0.2 fF/μm. Construct a π-model for the wire.   (8 Marks)

3.

a) Illustrate the problem of monotonicity in dynamic CMOS circuits. How it can be eliminated. (6 Marks)

b) Design a 3-input BiCMOS NAND gate. Label the transistor widths. What is the logical effort? (12 Marks)

OR

4.

a) Design a multi output domino logic to implement the following functions.

Y1=A+B

Y2=C (A+B)

Y3=D+C (A+B) (10 Marks)

b) With a neat sketch, discuss SOI and effect of floating body voltage. (8 Marks)

5.

a) Design the transistor level full adder circuit. (9 Marks)

b) Sketch and explain the basic design aspects of barrel shifter. (9 Marks)

OR

6.

a) Describe with example in detail the principle behind booth encoding. (12 Marks)

b) Design 6T SRAM cell. How read and write operation is performed. (6 Marks)