C

APJ Abdul Kalam Technological University

Ernakulam II Cluster

First Semester M.Tech Degree Examination December 2017

05EC 6005 ADVANCED DIGITAL DESIGN

Time: 3 hrs. Max. Marks: 60

1) a) Draw a state diagram for an FSM that has an input X and an output Y. Whenever X changes from 0 to 1, Y should become 1 for two clock cycles and then return to 0 even if X is still 1. (4 Marks)

b) What are ASM Charts? Realize the following ASM in figure 1 using D Flip-Flops.

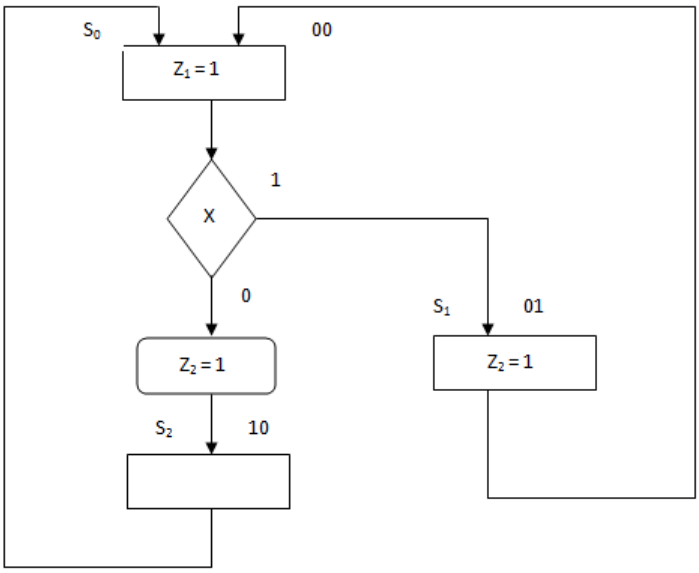

Figure 1

(8 Marks)

2) a) Use magnitude comparators and logic to design a circuit that outputs 1 when an 8-bit input 'a' is in between 75 and 100(both numbers inclusive). (6 Marks)

b) Design an ALU with two 8 bit inputs A and B, and control signals x, y and z. The ALU should support the operations in the table below. Use an 8-bit adder and an arithmetic logic extender

Inputs			Operation
x	y	z	
0	0	0	S = A – B
0	0	1	S = A + B
0	1	0	S = A * 8
0	1	1	S = A / 8
1	0	0	S = A NAND B (bitwise NAND)
1	0	1	S = A XOR B (bitwise XOR)
1	1	0	S = Reverse A (bit reversal)
1	1	1	S = NOT A (bitwise complement)

(6 Marks)

3) a) Design a laser- based distance measurement system, where a laser is pointed at the object of interest. The laser 's' briefly turned on and a timer is started. The laser light, travelling at the speed of light, travels to the object and reflects back. A sensor detects the reflection of the laser light, causing the timer to stop. Knowing the time T taken by the light to travel to the object and back, distance can be calculated. Use RTL design process. (12 Marks)

b) Compose a 16x1 MUX from 2x1 MUXs. (6 Marks)

OR

4) a) Determine the register-to-register critical path and the longest path delay for the circuit given in figure 2. Assume no wire delay, and the following component delays: Multipliers take 5 ns, Adders take 2 ns, Multiplexers take 1ns. Based on the longest path delay obtained, what should the frequency of this circuit be? (6 Marks)

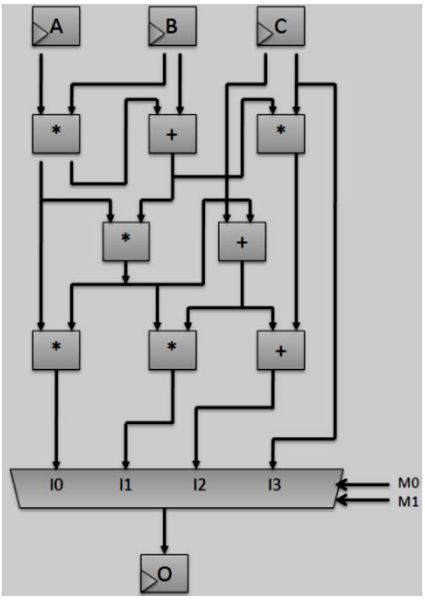

Figure 2

b) Compose a 4x16 decoder with enable from 2x4 decoders with enable. (6 Marks)

c) Summarize the main differences between DRAM and SRAM memories. (6 Marks)

5) a) Compare Moore and Mealey FSM. Design an FSM using mealey and moore model for a wrist watch that can perform the following operations a) display present time, b) set alarm c)display date d)act as a stop watch.The FSM should sequence to the next register, in the order listed above, each time a button b is pressed (assume b is synchronized with the clock as to be high for only 1 clock cycle on each unique button press). The FSM should set an output p to 1 each time the button is pressed, causing an audible beep to sound. (12 Marks)

b) Reduce the number of states for the FSM given in figure 3.

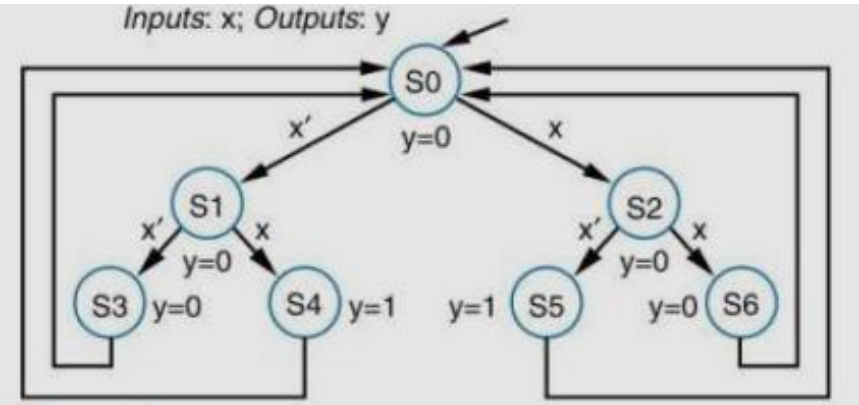

Figure 3

(6 Marks)

OR

6) a) Define state encoding. Discuss the various methods of state encoding. (8 Marks)

b) Design a circuit that repeatedly generates the output sequence 0,1,1,1. Encode the states using minimal binary encoding and one hot encoding and compare the size and delay.

(10 Marks)

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