E

APJ Abdul Kalam Technological University

Ernakulam II Cluster

First Semester M. Tech Degree Examination, December 2017

05EC 6011 – FPGA BASED SYSTEM DESIGN

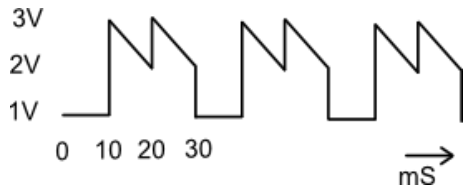
Time: 3 hrs Max. Marks: 60

I.

a) Design a 4bit gate level comparator and develop test bench program. [6 Marks]

b) Write Verilog code to find largest odd number form three 8bit inputs. If odd numbers are not available it should be indicated by a flag. [6 Marks]

II. Design an FSM based waveform generator with the following pattern. 12bit output from the generator represents data input to a 12bit DAC with 0 to 3.3V analog output range. [12 Marks]



III.

a) Design a UART transmitting and receiving system to accept bytes with 300 baud rate and transmit bit reversed input data. [14 Marks]

b) Write Verilog code for UART receiver with parity error detection output. [4 Marks]

OR

IV.

a) Describe a method to incorporate memory modules into a design? [4 Marks]

b) Design a system to perform the following operations on a 64KB x 8bit asynchronous RAM connected to FPGA. The operations are Clear all locations, fill all locations by a constant data and fill all locations by the pattern of 8bit up counter. There should be control inputs to select the operation. [14 Marks]

V.

a) Design a system to display a box filled with red color on VGA display. [12 Marks]

b) Write Verilog code for pixel generation of a font display circuit. [6 Marks]

OR

VI.

a) Draw timing diagrams of VGA synchronization and show timing calculation. [4 Marks]

b) Design a system to display the pattern “ABCD” on VGA screen. [14 Marks]