Exam Slot → **B**

APJ Abdul Kalam Technological University

First Semester M.Tech Degree Examination January 2016

Ernakulam II Cluster

ELECTRONICS COMMUNICATION ENGINEERING

Time : 3 hrs. 05EC 6003-CMOS DIGITAL DESIGN Max. Marks: 60

1.

a) Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions:

a) $Y = \overline{ABC + D}$

b) $Y = \overline{(AB + C) \cdot D}$

c) $Y = \overline{AB + C \cdot (A + B)}$ (6 Marks)

b) With a suitable example, discuss how the logical effort can be effectively used to estimate the multi-stage delay of a logical network.

(6Marks)

2.

a) Sketch the clock system architecture in a chip and explain the global clock generation.

(4 Marks)

b) Consider a 5 mm-long, 4 λ-wide metal wire. Use λ=90nm. The sheet resistance is 0.08 Ω/□ and the capacitance is 0.2 fF/μm. Construct a 3-segment π-model for the wire. An unit-sized (nMOS transistor width 4 λ) inverter drives an unit sized inverter at the end of the 5 mm wire. The gate capacitance is C = 2 fF/μm and the effective resistance is R = 2.5 kΩ · μm for nMOS transistors. Estimate the propagation delay using the Elmore delay model; neglect diffusion capacitance.

(8Marks)

3.

a) Why can't we cascade two dynamic gates? What is the solution? (6 Marks)

b) Sketch dynamic footed and un footed 3-input NAND and NOR gates. Label the transistor widths. What is the logical effort of each gate? (12 Marks)

OR

4.

a) Give the detailed account on principle and architectures used in NP Domino logic.

(10Marks)

b) With a neat sketch, discuss SOI and floating body voltage. (8 Marks)

5.

a) Sketch and explain a 4-bit carry-ripple adder using PG logic (9 Marks)
b) Sketch and explain the basic design aspects of array multiplier (9 Marks)

OR

6.

a) Describe in detail the principle behind 2's compliment array multiplication and booth encoding. (12 Marks)

b) Describe various serial access memories. (6 Marks)