C

APJ Abdul Kalam Technological University

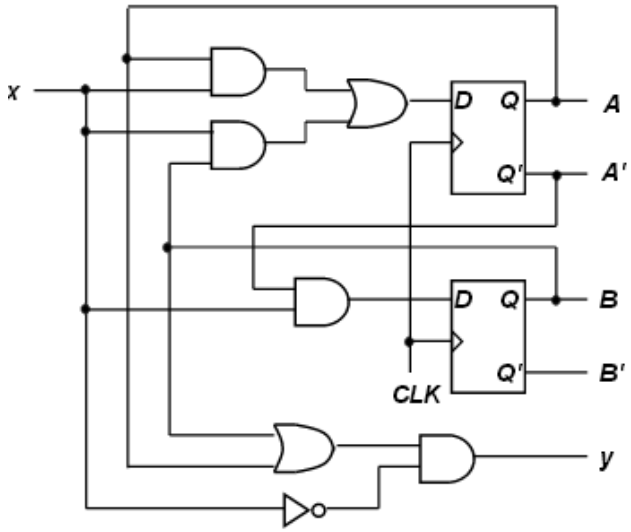
First Semester M.Tech Degree Examination February 2016

Ernakulam II Cluster

ELECTRONICS AND COMMUNICATION ENGINEERING

Time: 3 hrs. **05EC 6005 – ADVANCED DIGITAL DESIGN** Max. Marks: 60

1. a) Analyze the circuit shown in Fig.1 and construct the excitation table, transition table, state table and state diagram.

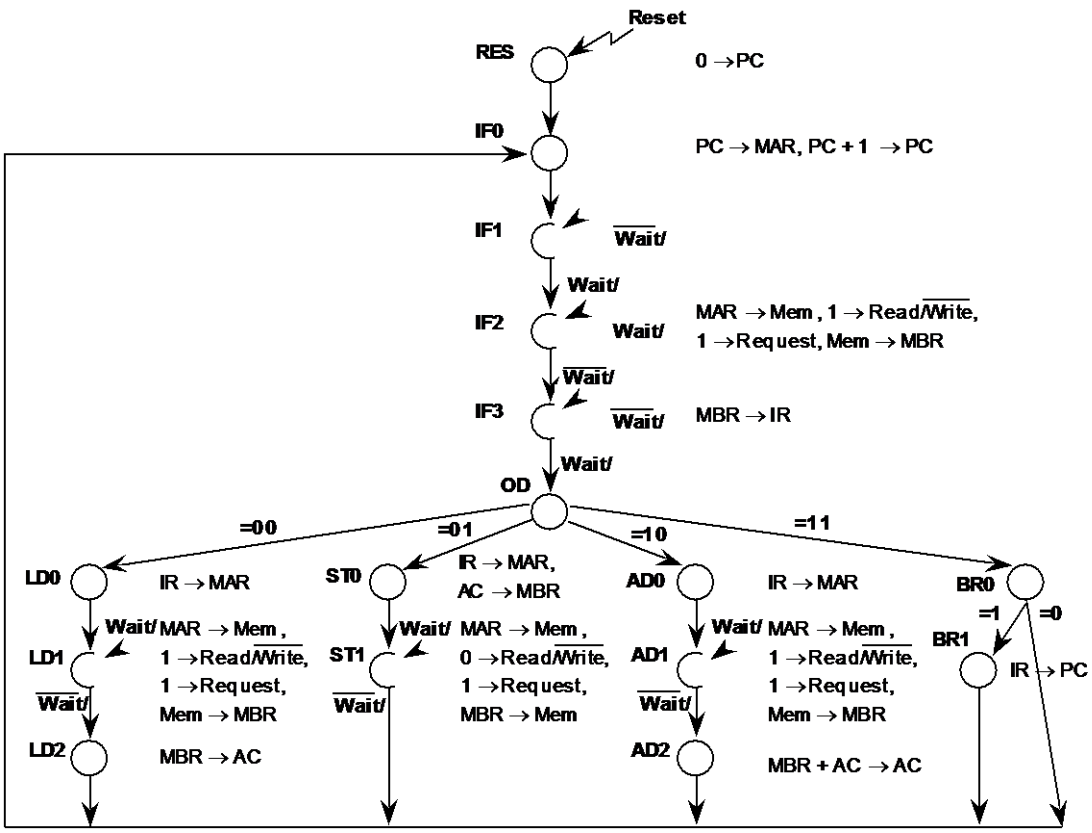


b) Obtain a minimal state table for a clocked synchronous sequential network having a single input line x, in which the symbols 0 and 1 are applied and a single output line z. An output of 1 is to be produced if and only if the three input symbols following two consecutive input 0's consist of at least one 1. At all other times the output is to be 0. An example of input/output sequences that satisfy the conditions of the network specifications is:

x: 0100010010010010000000011

z: 0000001000000100000000001 (6+6=12 Marks)

2 a) What are Time States? Generate the time states for the given state diagram. (6 Marks)



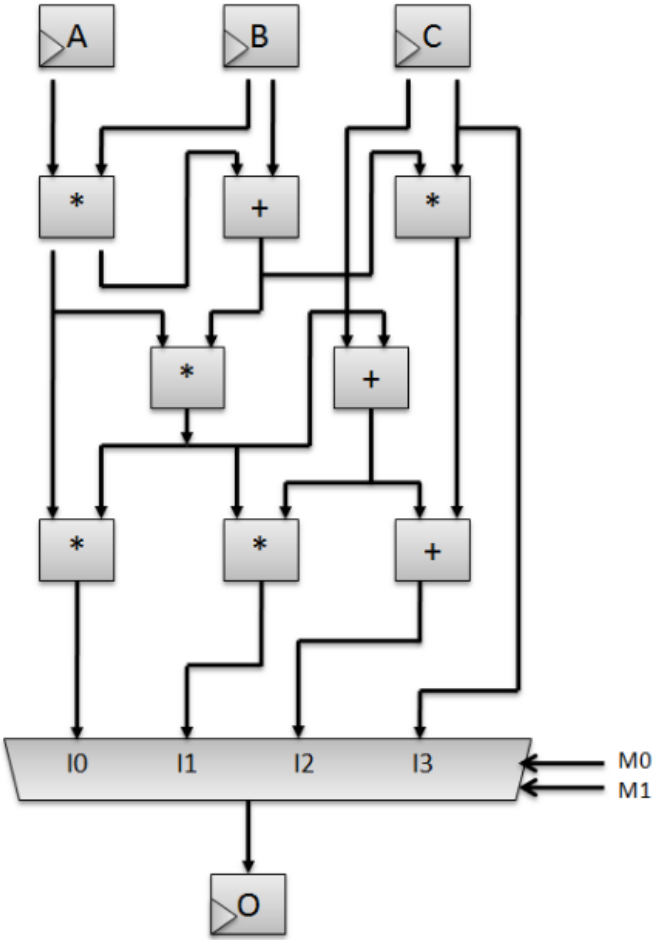
b) Draw the state diagram of a six state UP/Down Counter. Resolve the design using FSM decomposition. (6 Marks)

3 a) Determine the register-to-register critical path and the longest path delay for the circuit.

Assume no wire delay, and the following component delays:

Multipliers take 5 ns ,Adders take 2 ns , Multiplexers take 1ns .Based on the longest path delay obtained, what should the frequency of this circuit be?

(6 Marks)



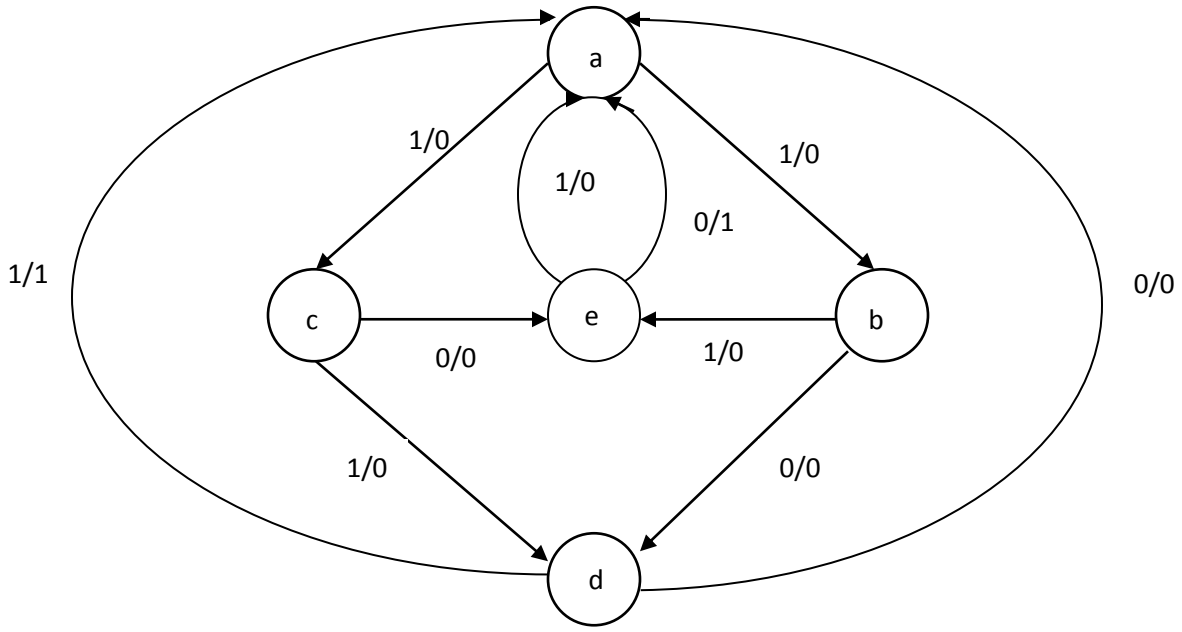
b) By using Hierarchy concept compose a 1024 x 8 ROM using only 512 x 4 ROMs .Also explain the types of ROMs and its advantages (12 Marks)

OR

4. a) Design the data path architecture of an 8 word 16-bit queue .Create an FSM describing the queue controller ,care full attention to correctly setting the full and empty output. (10 marks)

b) Introduce the concept of behavioral level design with the example of SAD for video compression. Explain HLSM templates for each assignment in C-code and design the HLSM for SAD. (8 Marks)

5. Design a sequential circuit using D Flip-Flops for the state diagram given below. Use state assignment rules for assigning states and compare the required combinational circuit with random state assignment. (9+9=18 Marks)



OR

6. What is latency and throughput? A circuit with no pipelining is shown. Estimate the latency and throughput if two and three stage, pipelining are employed. (3+5+5+5=18 Marks)