E

APJ Abdul Kalam Technological University

First Semester M.Tech Degree Examination February 2016

Ernakulam II Cluster

ELECTRONICS AND COMMUNICATION ENGINEERING

Time : 3 hrs. **05EC 6011 - FPGA BASED SYSTEM DESIGN** Max. Marks 60

I 12 Marks

a) Design a multiplexed 7 segment LED display system with three segments. Assume input clock frequency is 100 MHz. [8]

b) Write Verilog code for parameterised Mod-m counter. [4]

II 12 Marks

a) Design an FSM based switch de-bouncing circuit. Assume that a free-running 15ms timer generates a one-clock-cycle enable tick signal. [6]

b) Design a 20 bit Fibonacci number generator circuit. [6]

III 18 Marks

a) Write Verilog code to implement UART transmitter. [6]

b) Draw the block diagram, ASMD chart and develop Verilog code of SRAM controller with three-cycle back-to-back operation. [12]

OR

IV 18 Marks

a) Design a UART receiving subsystem consisting of receiver, 9600 bits per second baud rate generator, and interface circuit. Assume clock frequency is 25 MHz. [15]

b) Draw the block diagram of a 256K-by-16 SRAM. [3]

V 18 Marks

a) Write Verilog code to design a pixel-generation circuit for a 128-by-128 bit map. [12]

b) Explain the concept of object-mapped pixel generation circuit. [6]

OR

VI 18 Marks

a) Draw timing diagrams of VGA synchronization, show timing calculation and develop Verilog code to implement VGA synchronization circuit. [12]

b) Write Verilog code for pixel generation of a font display circuit. [6]