B

APJ Abdul Kalam Technological University

First Semester M.Tech Degree Examination December 2016

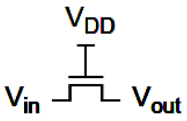
Ernakulam II Cluster

Time : 3 hrs. **05EC 6003-CMOS DIGITAL DESIGN** Max. Marks: 60

1.

a) Suppose *VDD* = 3.3 V and *Vt*= 0.4 V. Determine *V*out in Figure for the following. Neglect the body effect.

a) *V*in = 0V b) *V*in = 0.6 V c) *V*in = 3 V d) *V*in = 3.3 V.



(6 Marks)

b) With a suitable example, discuss how the logical effort can be effectively used to estimate the multi-stage delay of a logical network. (6 Marks)

2. a) Consider a 5mm long, 0.32µm widewire in a 180nm process. The sheet resistance is0.05ohms/square and the capacitance is 0.2fF/µm. Construct a π model for the wire. (4 Marks)

b) What is energy scavenging? (3 Marks)

c) What is electrostatic discharge protection? Draw the circuit for the same.

(5 Marks)

3. a) With figure, explain the principle of SOI? What are its advantages? (4 Marks)

b) Show how much time can be borrowed if a two phase latch is used for sequencing. (4Marks)

c) Implement g1=AB+C, g2= (AB+C) (D+E) using MODL logic gate. (10 Marks)

OR

4. a) What is the maximum delay constraint when a flip flop is used for sequencing.(5 Marks)

b) With neat circuit diagram describe the operational modes for a NORA Φ-section. (8 Marks)

c) How basic domino logic stage acts as a solution to the glitch problem. (5 Marks)

5. a) Sketch and explain a 4-bit carry-ripple adder using PG logic. (9 Marks)

b) Sketch and explain the basic design aspects of array multiplier. (9 Marks)

OR

6. a) Describe in detail the principle behind 2's compliment array multiplication and booth encoding. (12 Marks)

b) Describe various serial access memories. (6 Marks)