C

APJ Abdul Kalam Technological University

First Semester M.Tech Degree Examination December 2016

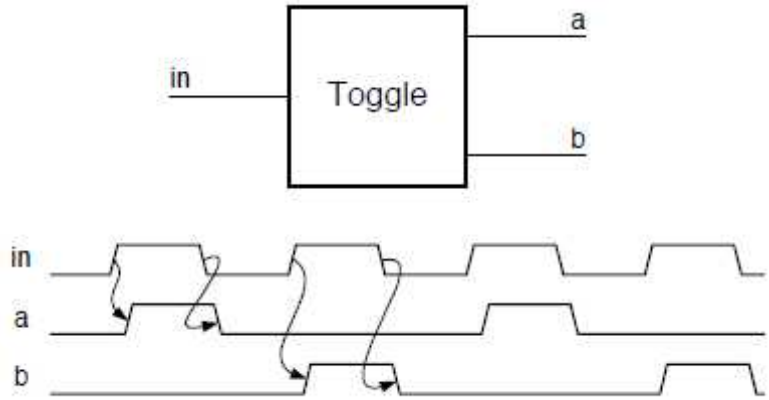
Ernakulum II Cluster

ELECTRONICS AND COMMUNICATION ENGINEERING

05EC 6005 Advanced Digital Design

Time: 3 hrs. Max. Marks: 60

1. (a) Design a fundamental-mode flow table for a toggle circuit that alternates pulses on its input 'in' between its two outputs 'a' and 'b' using the specifications shown graphically below.



(b) Design a clocked synchronous state machine using D Flipflops–a "combinational lock" state machine that activates an "unlock" output when a certain binary input sequence is received. It has one input, X, and two outputs, UNLK and HINT. The UNLK output should be 1 if and only if X is 0 and the sequence of inputs received on X at the preceding seven clock ticks was 0110111. The HINT output should be 1 if and only if the current value of X is the correct one to move the machine closer to being in the unlocked state(with UNLK =1). (6+6=12)

2. (a) Design an 8x32 two port (1 read, 1 write) register file.
   (b) Design a 4 bit array style multiplier. (6+6=12)
3. (a) Using the five-step controller design process, design and draw the final implementation of a soda machine dispenser controller. The soda dispenser has three inputs, **c**, **s**, and **a**. The 8 –bit input **s** represents the cost of each bottle of soda. The 1-bit input **c** is 1 for one clock cycle when a coin is inserted. The output **d** becomes 1

when the soda should be dispensed i.e. when the value of coins inserted into the soda dispenser is greater than or equal to **s**. The soda dispenser does not give change.

(b) Assuming an inverter has a delay of 1ns, all other gates have a delay of 2ns, and wires have a delay of 1ns, determine the critical path for a

i. 4x1 multiplexer.

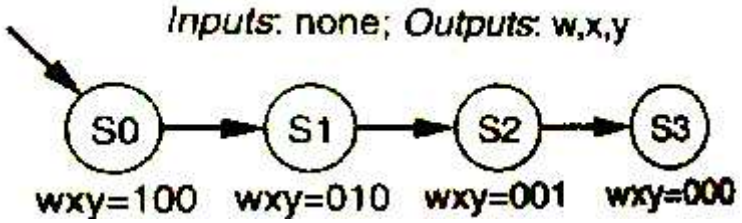
ii. 8 bit carry-ripple adder. (12+6=18)

OR

4. (a) Design the data path architecture of an 8 word 16-bit queue .Create an FSM describing the queue controller.

   (b) Compose a 2048x8 ROM using only 256x8 ROMs. (12+6=18)

5. (a) Compare the logic size (number of gate inputs) and the delay (number of gate delays) of a straightforward 2-bit binary encoding of the FSM given below using a 3-bit output encoding and with a one-hot encoding.

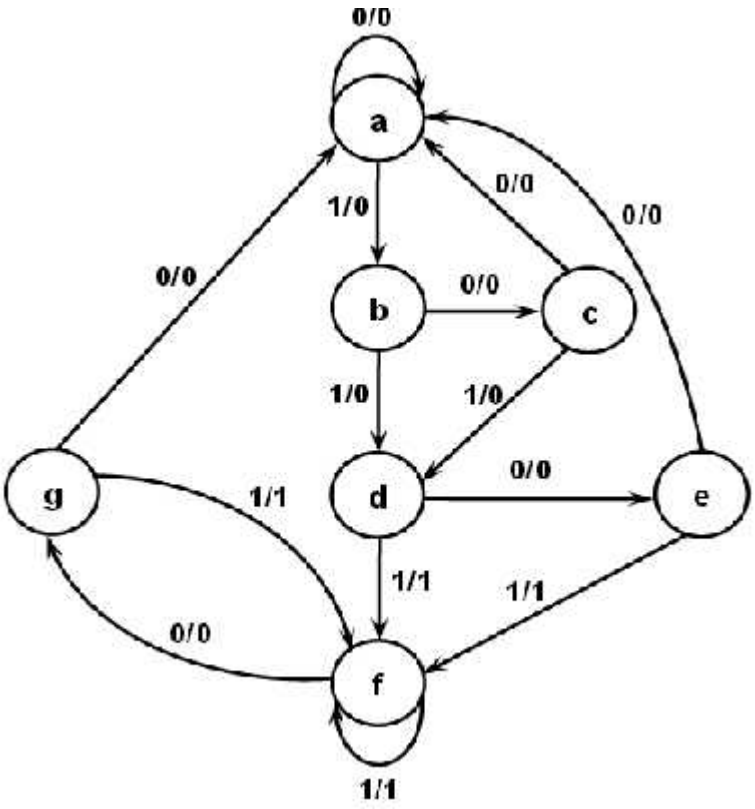


   (b) Design a 16 bit carry-select adder suing 4-bit ripple carry adders. Compute the size and delay of the circuit. (12+6=18)

OR

6. (a) Discuss in detail the optimizations and tradeoffs involved in RTL design.

   (b) Reduce the number of states for the FSM given below.



(12+6=18)