E

APJ Abdul Kalam Technological University

First Semester M.Tech Degree Examination December 2016

Ernakulam II Cluster

ELECTRONICS AND COMMUNICATION ENGINEERING

Time : 3 hrs. **05EC 6011 - FPGA BASED SYSTEM DESIGN** Max. Marks 60

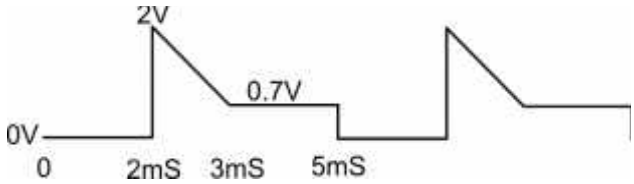
I 12 Marks

a) Design a circuit to rotate an 8-bit input to the right by 3 bits. [4]

b) Design a digital system to output all_equal, three_equal and two_equal from 4 N bit input variables. [8]

II 12 Marks

Eight bit output from FPGA is connected to R-2R ladder network based D to A converter. Develop a digital system to generate the given waveform. Assume that 8'hFF and 8'h00 will produce DAC outputs of 3.3V and 0V respectively.



III 18 Marks

An FPGA based system has 8 DIP switch inputs and 8 bit UART output. In every 60 seconds the status of the switch should be checked and an eight bit data should be transmitted corresponding to the status of the switches. Design block schematic, state diagram and write Verilog code with comments and explanation for each section. The baud rate of UART should be 4800. Assume input clock frequency is 50MHz.

OR

IV 18 Marks

a) Design a UART receiving subsystem consisting of receiver, baud rate generator, and interface circuit. [15]

b) Draw the block diagram of a 256K by 16 SRAM. [3]

V 18 Marks

Design a VGA interface module with 640 by 480 resolution. A vertical green bar of width 8 pixels should be displayed from top to bottom and its position on screen should be controlled by 2

push button switches named right and left. Assume clock frequency is 50MHz. Draw block schematic, state diagram and write Verilog code with comments and explanation for each section. [18]

OR

VI 18 Marks

a) Write Verilog code to design an object-mapped pixel-generation circuit for a ping pong game. [12]

b) Explain the concept of tile-mapped pixel generation circuit. Give an example. [6]