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APJ Abdul Kalam Technological University

Second Semester M.Tech Degree Examination May 2016

Ernakulam II Cluster

ELECTRONICS AND COMMUNICATION ENGINEERING
[VLSI & EMBEDDED SYSTEMS]
ELECTIVE-III

Time: 3 hrs. **05EC6034 LOW POWER VLSI DESIGN** Max. Marks 60

I 12 Marks

a) Explain physics of power dissipation in MOSFET devices. [8]

b) Give an account on power dissipation in CMOS. [4]

II 12 Marks

a) Give in detail the concept of Differential current logic with neat diagram. [6]

b) Express the Deep submicron device design issues with an example. [6]

III 18 Marks

a) With necessary figures, explain the concept of Low power SRAM. [10]

b) Give details the concept of Banked organization of SRAMs with an example. [8]

OR

IV 18 Marks

a) Give the details about reducing power in write driver circuits with neat diagram. [10]

b) Write a note on reducing power in sense amplifier circuits with an example. [8]

V 18 Marks

a) Formulate the adiabatic switching. [10]

b) Show the Adiabatic amplification with neat diagram. [8]

OR

VI 18 Marks

a) Sketch an adiabatic logic gates with neat block diagram. [10]

b) Draw the fully adiabatic sequential circuits with suitable figure. [8]