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APJ Abdul Kalam Technological University

Ernakulam II Cluster

Second Semester M.Tech Degree Examination May 2017

Time: 3 hrs. **05EC6034 - LOW POWER VLSI DESIGN** Max. Marks: 60

1. a) Explain Short circuit current in CMOS circuit. [8 Marks]

   b) Give an account of basic principles of low power design. [4 Marks]

2. a) Explain Differential current switch logic 1 and 3 with neat diagram. [6 Marks]

   b) Explain any two non clocked circuit design style. [6 Marks]

3. a) With a neat block diagram, explain the organization of SRAM [10 Marks]

   b) With neat diagram explain the concept of 6T SRAM cell and its operation. [8 Marks]

OR

4. a) Give the detailed concept of Banked organization of SRAMs with an example. [8 Marks]

   b) Give the details about reducing power in write driver circuits with neat diagram. [10 Marks]

5. a) Explain adiabatic charging. Derive the expression for energy dissipation. [10 Marks]

   b) With neat diagram, briefly explain adiabatic amplification. [8 Marks]

OR

6. a) Describe adiabatic logic gates with neat block diagram. [10 Marks]

   b) Explain about stepwise charging. [8 Marks]