APJ Abdul Kalam Technological University

Ernakulam II Cluster

Third Semester M.Tech Degree Examination December 2017

05EC7043- TESTING OF VLSI CIRCUITS

Time: 3 hrs   Max. Marks: 60

1. a) How testing is performed? What are the different types of Testing in VLSI circuit design?

[7 Marks]

   b) Write a short note on VLSI technology trends affecting testing.   [5 Marks]

2. a) Write a note on combinational testability measures.   [6 Marks]

   b) Explain compiled code and event driven simulation.   [6 Marks]

3. a) Enumerate major mode of operation provided by Boundary scan?   [6 Marks]

   b) Write short notes on:

      i) Weighted pseudo random pattern generator.

      ii) Cellular Automaton Pattern Generation   [12 Marks]

OR

4. a) Define BIST and briefly explain BIST process.   [10 Marks]

   b) Explain boundary scan test instructions.   [8 Marks]

5. a) Explain the basic principle of IDDQ testing.   [6 Marks]

   b) Briefly explain Path Delay Test.   [12 Marks]

OR

6. a) Explain IDDQ testing methods.   [8 Marks]

   b) Briefly explain ATPG.   [10 Marks]