B

APJ Abdul Kalam Technological University

Ernakulam II Cluster

Third Semester M.Tech Degree Examination December 2017

05EC7051- VLSI AND COMPUTER AIDED DESIGN

Time: 3 hrs.   Max. Marks: 60

Module 1

I.   a) Briefly explain the VLSI design cycle.   (6 Marks)

    b) With neat diagram explain the design rules for physical design automation. (6 Marks)

Module 2

II.   a) Discuss the types of placement problem.   (4 marks)

    b) Explain in detail the Kernighan – Lin partitioning algorithm with the help of the example given below. Initial partition should be done as shown in the figure. (8 Marks)
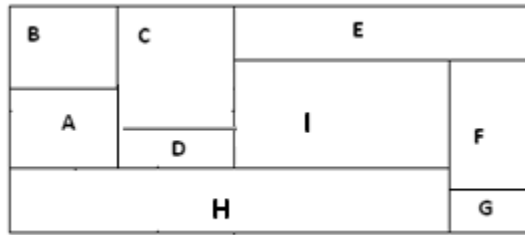

    ↳ initial partitioning
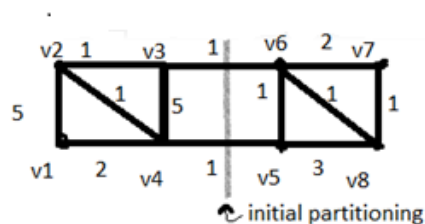
Module 3

III.   a) Describe the terminologies used in floor planning.   (6 Marks)

    b) What are the different methods of representing a floor plan? Explain each with the help of an example.

                                                                                         (12 marks)

OR

IV.   a) Draw the hierarchical floor plan representation for the example given below.

(6 Marks)

b). Explain with necessary diagrams shape function and floor plan sizing in floor planning.   (12 Marks)

Module 4

V.   a) What is global routing in standard cell layout. Discuss with the aid of pseudo code, the Rectilinear Steiner-tree algorithm used in global routing.   (12 Marks)

b) Differentiate between local routing and global routing.   (6 Marks)

OR

VI.   a) Explain the significance of area routing.   (12 Marks)

b) Write in detail about the taxonomy on VLSI routers.   (6 Marks)