A

APJ Abdul Kalam Technological University

Third Semester M.Tech Degree Examination December 2016

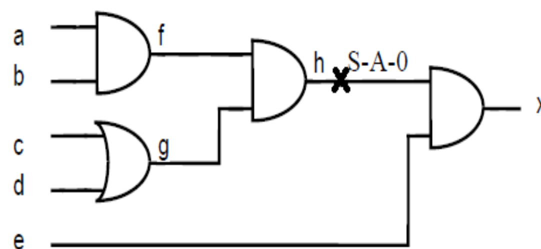
Ernakulam II Cluster

Time: 3 hrs. **05EC7043- Testing of VLSI Circuits** Max. Marks 60

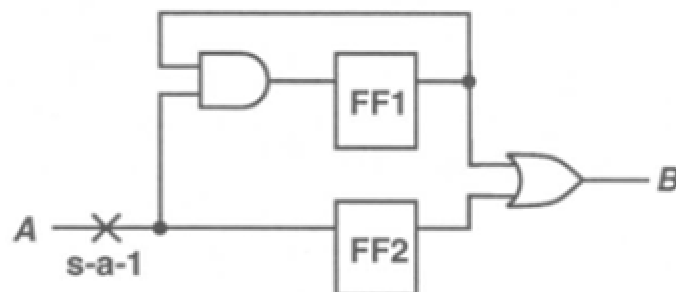
I. a) Explain any 6 fault models. [6 Marks]

b) Explain with an example equivalent fault collapsing and dominant fault collapsing. [6 Marks]

II a) Use D-ALG to perform ATPG for S-A-0 fault at line h in the circuit given below. [6 Marks]



b) Show that a test for the fault **A** S-A-1 in the circuit given below, cannot be obtained using the five valued logic. Obtain a test for this fault using nine valued logic. [6 Marks]



III. a) Explain the main idea of scan design method and scan design rules. [12 Marks]

b) Explain BIST process and BIST implementations [6 Marks]

OR

IV. a) How Scan test sequences are generated? [6 Marks]

b) How full scan design is automated? [6 Marks]

c) Draw the diagram of external-XOR standard LFSR with characteristics polynomial $f(x) = 1 + x + x^3$. [6 Marks]

V. a) Write Short notes on.

i) Stuck-At faults. ii) Inversion coupling faults. iii) State coupling faults.

iv) Neighbourhood pattern sensitive coupling faults. [12 Marks]

b) Explain how IDDQ test is performed. [6 Marks]

OR

VI .a) Discuss in detail about any two delay test methodologies. [10 Marks]

b) Explain the classifications of system test. [8 Marks]