B

APJ Abdul Kalam Technological University

Third Semester M.TechDegree Examination December 2016

Ernakulam II Cluster

ELECTRONICS AND COMMUNICATION ENGINEERING

05EC 7051 VLSI AND COMPUTER AIDED DESIGN

Time: 3 hrs. Max. Marks:60

Module 1

I. a) Briefly explain about physical design automation. (4 Marks)

b) Explain in detail Bellman Ford algorithm with the help of an example. (8 Marks)

Module 2

II. a) Discuss about different levels of placement. (4 marks)

b) Explain in detail the Kernighan – Lin partitioning algorithm with the help of a suitable example. (8 Marks)

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Module 3

III. a) Describe the problems of floor planning. (6Marks)

b) What are the different methods of representing a floor plan? Explain each with the help of an example. (12 Marks)

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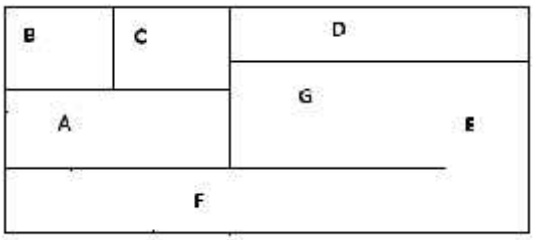
OR

IV. a) Draw the hierarchical floor plan representation for the example given below.



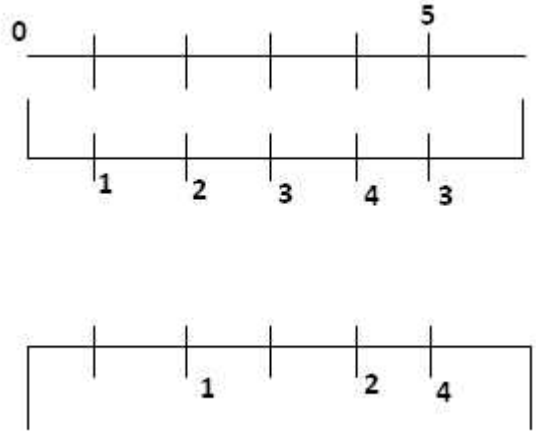
(6 Marks)

b) Explain with necessary diagrams shape function and floor plan sizing in floor planning. (12 marks)

Module 4

V. a) Differentiate between global routing and local routing. (6 marks)

b) Discuss in detail about robust channel routing algorithm with the help of the example given below.



(12 marks)

OR

VI. a) State different types of local routing problems. (6 marks)

b) With the help of an example explain in detail the global routing algorithm. (12 marks)