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APJ Abdul Kalam Technological University

Ernakulam Cluster II

Second Semester M.Tech Degree Examination May 2017

05 CS6026-ADVANCED COMPUTER ARCHITECTURE

Time: 3 hrs. Max. Marks: 60

1.
   a) Distinguish between fixed and variable length encoding of instructions. (6 Marks)
   b) Illustrate the various Memory Addressing Modes. (6 Marks)

2.
   a) What are the Compiler Optimizations techniques used to reduce Cache Miss Rate? (6 Marks)
   b) Explain the concept of Pentium Page Tables. Explain Address translation with a page table. (6 Marks)

3.
   a) How does the 1 Bit and 2 Bit predictors help in Branch prediction? How can they be used in Pipelining? (6 Marks)
   b) Explain how to perform Dynamic scheduling with scoreboard in MIPS Processor. (12 Marks)

OR

4.
   a) Explain the architecture of MIPS R4000 Pipeline. (9 Marks)
   b) How can the data hazard be avoided? Explain the strategy used for avoiding data hazards for the following set of instructions: (9 Marks)

LD R1, 45, (R2)	LD R1, 45, (R2)
ADD R5, R1, R7	DADD R5, R6, R7
DSUB R8, R6, R7	DSUB R8, R1, R7
OR R9, R6, R7	OR R9, R6, R7
(a)	(b)

5.

a) What is the role of Memory Banks in Vector Processing?

The largest configuration of a Cray T90 (Cray T932) has 32 processors, each capable of generating 4 loads and 2 stores per clock cycle. The processor clock cycle is 2.167 ns, while the cycle time of the SRAMs used in the memory system is 15 ns. Calculate the minimum number of memory banks required to allow all processors to run at full memory bandwidth. (6 Marks)

b) One of the problems in vector processor is that the size of all the vector operations depends on vector length which is sometimes longer than the maximum length. Describe how to solve this problem with an example. (6 Marks)

c) Explain the Fermi GPU Architecture. (6 Marks)

OR

6.

a) Explain the different concepts in Vector Processing. (6 Marks)

b) Compare between multimedia SIMD computers and GPUs. (6 Marks)

c) Implement DAXPY problem using VMIPS. (6 Marks)