F 6878 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2017

Third Semester

Branch : Computer Science and Engineering/Information Technology

EN 010 301 B—ENGINEERING MATHEMATICS—II [CS, IT]

(New Scheme—2010 Admission onwards)

[Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Define Tautology and contradictions ?
2. What are the properties of a congruence relation ?
3. Define Binary Relation, Give example for a binary relation ?
4. Explain the properties of a lattice.
5. Define complete graph ? Give an example.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Construct the truth table for the following propositions ?
   (a) $p \vee \sim p$.
   (b) $\sim (p \wedge \sim q)$.
7. S.T. that the numbers 25 and 37 are relatively prime using Euclidean algorithm.
8. Consider the 'subset' relation $\subseteq$ on the set $P(\{1, 2, 3\})$, that is for all sets U and V in $P(\{1, 2, 3\})$ $U \subseteq V \Leftrightarrow \forall x$, if $x \varepsilon U$ then $x \varepsilon V$ construct a Hasse diagram for this relation.
9. Define Algebraic system ? What are its general properties ?
10. Define Tree ? What are its properties ?

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) S.T. $\sim(p \vee (\sim p \wedge q))$ and $\sim p \wedge \sim q$ are logically equivalent ?

(b) S.T. $(p \wedge q) \rightarrow (p \vee q)$ is a tautology.

(6 × 2 = 12 marks)

Or

12. (a) Define the terms : proposition, conjunction, disjunction and negation with examples.

(b) Define the laws of algebra of propositions ?

(6 × 2 = 12 marks)

13. (a) Using Fermat's Theorem find 3^{12} mod 11 ? (3 marks)

(b) Using pigeonhole principle, show that if any *five* numbers from 1 to 8 are chosen, then two of them will add upto ?

(9 marks)

Or

14. (a) If $A = \{1, 2, \ldots n\}$ show that any function from A to A which is one to one must also be onto and conversely.

(9 marks)

(b) using Euler's theorem find 20^{62} mod 77. (3 marks)

15. (a) Define is relation R on Z by aRb if $4a + b$ is a multiple of 5. Show that R defines an equivalence relation on Z.

(9 marks)

(b) Define partial order on a set. (3 marks)

Or

16. (a) Let $(A, \leq)$ be a poset and $a, b \in A$ can a and b have two least upper boomds ? Explain.

(9 marks)

(b) Define Equivalence Relations. (3 marks)

17. Explain the following in detail :—

(a) Complete lattice.

(b) Bounded lattice.

(c) Complemented lattice.

(3 × 4 = 12 marks)

Or

18. Let p and q are elements in a bounded distributed lattice $(L, \leq \wedge, \vee)$ and if p^T is the complement of p, then show that $p \vee (p^T \wedge q) = p \vee q$ and $p \wedge (p^T \vee q) = p \wedge q$.

(12 marks)

19. (a) P.T. A graph G is hamiltonian iff its closure ((G) is Hamiltonian. (6 marks)

(b) P.T. the graphs $k_{n,n}$ are Hamiltonian for every $n \geq 2$. (6 marks)

Or

20. Explain in detail with example :

(a) Weighted Graph.

(b) Path.

(c) Cycle.

(d) Iso morphic graph.

(4 × 3 = 12 marks)

[5 × 12 = 60 marks]

F 6907 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2017

Third Semester

Branch : Computer Science and Engineering/Information Technology

CS 010 305/IT 010 304—SWITCHING THEORY AND LOGIC DESIGN [CS, IT]

(New Scheme—2010 Admission onwards)

[Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. What are the applications of grey code.
2. Differentiate between PAL and PLA.
3. Draw the logic diagram of SR latch.
4. Differentiate combinational and sequential circuits.
5. What is fundamental mode operation in Asynchronous circuits ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. State distributive law and Convert the hex number F3A2 to binary and octal.
7. Draw the internal circuit diagram of a 8 × 1 multiplexer and give the truth table.
8. Write short note on design of clocked sequential circuits using state equations.
9. Define BCD counter. Draw the logic diagram of 4-bit Binary counter with parallel load.
10. Write short note on fault tolerance in combinational circuits.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. Design and implement :

    (i) Three bit binary-to-gray converter ; and

    (ii) Four bit gray-to-binary converter.

Or

12. Convert to Canonical forms :

    (i) $F_1(X, Y, Z) = X\,Y + Z$.

    (ii) $F_2(X, Y\,Z) = (X + Y')(X' + Z)$.

    (iii Using K map, simplify the following expression and implement them using N A N D gates

    $F_1(A, B, C, D) = \sum m(1, 5, 6, 7, 11, 12, 13) + \sum d\ (10, 15)$.

13. Explain in detail about full order and realize 2 bit binary parallel with logic diagram and truth table.

Or

14. (i) Implement the following functions using PLA having 3 inputs, 4 product terms and 3 outputs.

$F_1(A, B, C) = \sum m(3, 5, 6, 7)$; $F_2(A, B, C) = \sum m(0, 2, 5, 7)$; $F_3(A, B, C) = \sum m(1, 2, 5, 7)$;

    (ii) Implement the function using only one 8 × 1 multiplexer where the binary inputs A, B, C are connected to the selection lines S_0, S_1 and S_2 respectively.

$F(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 9, 11, 13)$.

(8 + 4 = 12 marks)

15. A sequential circuit has three D flip flops A, B, C and one input x. It is described by the following flip flop input functions T_A = (BC' + B'C) X + (BC + B' C') X' ; T_B = A + B ; D_C = B. the output Y = AB + X. Derive the state table. Draw the state diagram for X = 1.

Or

16. With neat sketch explain the working of Master Slave JK flip flop.

17. Design a three-bit synchronous counter that goes through the following states 1, 2, 4, 6, 0... Use T flip flops for realisation.

Or

18. Describe shift register. Explain the various types of shift registers.

19. What is hazard and essential hazard ? Explain the hazards in combinational circuits and sequential circuits.

Or

20. Explain with Boolean difference method for fault diagnosis in digital circuits.

(5 × 12 = 60 marks)