Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FOURTH SEMESTER B.TECH DEGREE EXAMINATION, APRIL 2018

Course Code: CS202

Course Name: COMPUTER ORGANIZATION AND ARCHITECTURE (CS, IT)

Max. Marks: 100 Duration: 3 Hours

PART A
Answer all questions, each carries 3 marks Marks

1 With a neat diagram, explain the internal architecture of the CPU. (3)

2 What are condition codes? List the different condition codes. (3)

3 Prove that the worst case delay through an $n \times n$ array multiplier is $6(n-1)-1$ gate delays. (3)

4 Enumerate the sequence of actions involved in executing an unconditional branch instruction. (3)

PART B
Answer any two questions, each carries 9 marks

5 a) With the help of examples, explain the different addressing modes. (5)

b) Register R6 is used in a program to point to the top of a stack containing 32-bit numbers. Write a sequence of instructions using the Index, Autoincrement, and Autodecrement addressing modes to perform each of the following tasks: (4)
(*a*) Pop the top two items off the stack, add them, then push the result onto the stack.
(*b*) Copy the fifth item from the top into register R3.
For each case, assume that the stack contains ten or more elements.

6 a) With the help of a diagram, describe the datapath inside the processor. (5)

b) Discuss the different ways in which the return address can be saved during a subroutine call. Which of these methods support subroutine nesting? Justify your answer. (4)

7 a) Write down the sequence of actions needed to fetch and execute the instruction: (3)

Store R6, X(R8).

b) Multiply each of the following pairs of signed 2's-complement numbers using the Booth algorithm. In each case, assume that A is the multiplicand and B is the multiplier. (6)
i) A = 001011 and B = 011011
ii) A = 000111 and B = 000111

PART C
Answer all questions, each carries 3 marks

8 Explain the functions of interface circuits. (3)

9 List and describe the registers in a DMA interface. (3)

10		The cache block size in many computers is in the range of 32 to 128 bytes. What would be the main advantages and disadvantages of making the size of cache blocks larger?	(3)
11		What is flash memory?	(3)

PART D

Answer any two questions, each carries 9 marks

12	a)	With a diagram, explain the PCI bus.	(5)
	b)	Write a note on the packet type formats of USB.	(4)
13	a)	What are interrupts? List the sequence of steps following an interrupt request.	(5)
	b)	Describe semiconductor RAM memories.	(4)
14	a)	With the help of an example, explain the different cache mapping function	(6)
	b)	A computer system has a main memory consisting of 1M 16-bit words. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block. Calculate the number of bits in each of the Tag, Set, and Word fields.	(3)

PART E

Answer any four questions, each carries 10 marks

15	a)	Discuss shift and conditional control micro operations.	(7)
	b)	An 8-bit register A has one input x. The register operation is represented symbolically as P: $A_7 \leftarrow x$, $A_i \leftarrow A_{i+1}$ $i = 0,1,2,3 \ldots 6$. What is the function of the register?	(3)
16		Compare vertical and horizontal microinstruction formats, giving examples.	(10)
17		With a diagram, explain how control signals are generated using hardwired control.	(10)
18		Describe the purpose of microprogram sequencing. How is it carried out?	(10)
19		Draw the block diagram for the hardware that implements the following statement x + yz: AR ← AR + BR where AR and BR are two n-bit registers and x, y, and z are control variables. Include the logic gates for the control function. (The symbol + designates an OR operation in a control or Boolean function and an arithmetic plus in a micro operation.)	(10)
20		Explain the design of status register.	(10)

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