

Reg. No. _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION, JANUARY 2017

Course Code: **IT201**Course Name: **DIGITAL SYSTEM DESIGN (IT)**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer any 2 questions. Each question carries 15 marks.*

1)

- a) Convert 203.52_{10} to binary and hexadecimal. (5)
- b) Divide binary numbers 11011.1_2 by 101_2 (4)
- c) Subtract 46.5_{10} from 125.5_{10} using 2's complement arithmetic. (3)
- d) Compare 1's and 2's methods of representations. (3)

2)

- a) Reduce following expressions by using K-map. (9)

$$A\bar{B}C + \bar{B} + B\bar{D} + AB\bar{D} + \bar{A}C$$

- b) Implement following expression in NOR logic. (4)

$$AB + \bar{C}D(\bar{B} + \bar{D})$$

- c) Convert following expressions to minterm. (2)

$$ABCD + AB\bar{C} + ACD$$

3)

- a) Reduce following expressions by using K-map (9)

$$(B + \bar{C})(A + B + \bar{D})(\bar{A} + C + D)(B + C + D)$$

- b) Without reducing, convert following expression to NAND logic. (4)

$$C\bar{D}(A + B) + D(A + BC)$$

- c) Convert following expressions to maxterm. (2)

$$(A + \bar{B} + C)(B + C + \bar{D})(\bar{A} + \bar{B} + D)$$

PART B

Answer any 2 questions. Each question carries 15 marks.

- 4)
- a) Design full adder circuit and implement with both basic logic gates and with NAND logic gates. (10)
 - b) Draw and explain 4 bit BCD adder circuit with correction detector circuit. (5)
- 5)
- a) Design full subtractor circuit and implement with both basic logic gates and with NAND logic gates. (10)
 - b) Draw and explain 4 bit adder/subtractor circuit (5)
- 6)
- a) Write in detail about the following flip flop characteristics: propagation delay time, maximum clock frequency, power dissipation and set-up time. (8)
 - b) Design a monostable multivibrator by using NOR gate and inverter. Explain its working with the help of waveforms. (7)

PART C

Answer any 2 questions. Each question carries 20 marks.

- 7)
- a) Design a 3 bit up/down synchronous counter and implement by using JK flip flop. Explain the working with state diagram. (12)
 - b) Discuss 4 bit SERIAL-IN SERIAL-OUT RIGHT SHIFT shift register using JK and SR flip flops with the help of timing diagram. (8)
- 8)
- a) Design and implement a counter that goes through 1,3,4,6,10,12,14,2,1,3,4... using T flip flops by eliminating lock out (in the case of invalid states, go to initial state) (12)
 - b) Draw and explain a 4 bit ring counter with state diagram and timing diagram. Use JK flip flops. (8)
- 9)
- a) Discuss Booth multiplication algorithm. Multiply 7 and -3 using this algorithm. (12)
 - b) Write a short notes on mask-programmed ROM and programmable ROM (8)
