D

APJ Abdul Kalam Technological University

Ernakulam II Cluster

Second Semester M.Tech Degree Examination April/May 2018

05 CS6026 - ADVANCED COMPUTER ARCHITECTURE

Time: 3hrs Max Marks: 60

I. a) Compare and contrast between the various instruction set architectures(ISA) (6 Marks)

b) State Amdhal's Law. If a program currently takes 100 seconds to execute and loads and stores account for 20% of the execution times, how long will the program take if loads and stores are made 30% faster? (6 Marks)

II. a) A computer with a L1 cache and L2 cache memory hierarchy with the following parameters: Processor Clock Frequency = 1 GHz ;

Hit Time L1 = 1 clock cycle; Hit Rate L1 = 95%;

Hit Time L2 = 5 clock cycles; Hit Rate L2 = 90%;

Miss Penalty L2 = 15 clock cycles;

Memory Accesses Per Instruction = 78% ; CPI exec = 3

1. How much is the Global Miss Rate for Last Level Cache?
2. How much is the Global Miss Rate for Last Level Cache?
3. How much is Miss Penalty L2?
4. How much is Miss Penalty L1? (8 Marks)

b) Where can a block be placed in the upper level? Explain? (4 Marks)

III. a) Discuss the strategies used to reduce the branch miss penalties. (4 Marks)

b) Discuss how to detect and handle hazards in the longer latency pipelines (8 Marks)

c) Consider an unpipelined machine with five stages (Instruction Fetch, Instruction Decode/ Register Fetch, Execute/Address Calculation, Memory Access and Write Back). Assume that it has 11-ns clock cycles. The machine uses four cycles for ALU operations and branches and five cycles for memory operations. Assume that the relative frequencies of these operations are 45%, 15% and 40% respectively. Pipelining the machine adds 1-ns of overhead to the clock. Find out how much speedup we will gain in the instruction execution rate. You can ignore any latency impact. (6 Marks)

OR

VI. a) Discuss how pipeline is implemented in MIPS with detailed operations at each stage (7 Marks)

b) Suppose the branch frequencies (as percentage of all instructions) are as follows:

Conditional branches 15 %

Jumps and calls 1 %

Conditional branches 60 % are taken. We are examining a four-deep pipeline where the branch is resolved at the end of the second cycle for unconditional branches and at the end of the third cycle for conditional branches. Assuming that only the first pipe stage can always be done independent of whether the branch goes and ignoring other pipeline stalls, how much faster would the machine be without any branch hazards? (7 Marks)

c) The problem in long running instruction is that the instructions are completing in a different order than they were issued. What are the approaches to deal with this situation? (4 Marks)

V a) Discuss the significance of multiple lanes in Vector Architecture. (6 Marks)

b) Compare and contrast between vector processors and GPUs. (6 Marks)

c) Consider the following loop:

```
for (i = 0; i < n; i=i+1)
A[K[i]] = A[K[i]] + C[M[i]];
```

where K and M and index vectors to designate the nonzero elements of A and C. Assume that A and C are sparse matrices, suggest a method to vectorize it and write the vectorized code sequence for the above code. (6 Marks)

OR

VI. a) What are the data dependencies between the statements S1 and S2 in the loop? (6 Marks)

```
for (i=1; i<=100; i=i+1) {
        A[i+1] = A[i] + C[i];  /*  S1 */
        B[i+1] = B[i] + A[i+1];}  /* S2 */
         }
```

b) Detect loop carried dependence using gcd test for the following code? (8 Marks)

```
for (i=1; i<=100; i=i+1)
{
        x[2*i+3] = x[2*i] * 5.0;
}
```

c) Elaborate on GPU instruction set architecture. (4 Marks)