E

APJ Abdul Kalam Technological University

Ernakulam II Cluster

Second Semester M.Tech Degree Examination April/May 2018

05EC6034 - LOW POWER VLSI DESIGN

Time: 3 hrs. Max. Marks: 60

1. a) Explain the sources of CMOS leakage current. . [8 Marks]

   b) Explain the needs for Low power VLSI chips. [4 Marks]

2. a) Describe how to minimize the short channel effects. [6 Marks]

   b) What are the low voltage circuit design techniques? [6 Marks]

3. a) With a neat block diagram, explain the organization of SRAM. [10 Marks]

   b) With neat diagram explain the concept of 6T SRAM cell and its operation. [8 Marks]

OR

4. a) Give the methods of reducing voltage swings on bit lines. [10 Marks]

   b) Explain the operation of sense amplifier circuit with neat figures. [8 Marks]

5. a) Explain fully adiabatic sequential circuits. [10 Marks]

   b) Discuss about one stage adiabatic buffer. [8 Marks]

OR

6. a) Explain adiabatic switching and charging. [10 Marks]

   b) Explain about stepwise charging. [8 Marks]