F 3082 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science/Information Technology

ENGINEERING MATHEMATICS II—(R,T)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Answer any **one** *full question from each module.*
Each full question carries 20 *marks.*

Module 1

1. (a) Let m and n be integers. Prove that $n^2 = m^2$ if and only if n is m or n is $-m$.

   (b) "If there was a ball game, then travelling was difficult. If they arrived on time, then travelling was not difficult. They arrived on time. Therefore, there was no ball game". Show that these statements constitute a valid argument.

Or

2. (a) Construct the truth table for $(P \to Q) \wedge (Q \to P)$.

   (b) Show that $p \to q, \sim (q \vee r) \Rightarrow \sim p$.

   (c) Symbolize : "All the world loves a lover".

Module 2

3. (a) Show that one of any m consecutive integers is divisible by m.

   (b) Let R be a binary relation on the set of all strings of 0s and 1s such that $R = \{(a, b) | a$ and b are strings that have the same number of 0s$\}$. Is R reflexive ? Symmetric ? Antisymmetric ? Transitive ? An equivalence relation ? A partial ordering relation.

Or

4. (a) Let R be a binary relation from A to B. The converse of R, devoted R^{-1}, is a binary relation from B to A such that $R^{-1} = \{(b, a) | (a, b) \in R\}$ Let R_1 and R_2 be binary relations from A to B.

   Is it true that $(R_1 \cup R_2)^{-1}$ $R_1^{-1} \cup R_2^{-1}$?

Turn over

(b) Explain Pigeonhole principle. using it, show that if any 5 numbers from 1 to 8 are chosen, then two of them will add upto 9.

Module 3

5. (a) Show that for any elements a, b, c in a modular lattice

$(a \vee b) \wedge c = b \wedge c$ implies $(c \vee b) \wedge a = b \vee a$.

(b) Show that a lattice $(A, \leq)$ is distributive if and only if for any elements $a, b\ c$ in A,

$(a \wedge b) \vee (b \wedge c) \vee (c \wedge a) = (a \vee b) \wedge (b \vee c) \wedge (c \vee a)$.

Or

6. (a) Show that $(a * b)' = a' \oplus b'$ and $(a \oplus b)' = a' * b'$ hold in a complemented, distributive lattice.

(b) Show that the lattice $\langle S_n, D \rangle$ for n = 216 is isomorphic to the direct product of lattices for n = 8 and n = 27.

Module 4

7. (a) Find a simple expression for the generating function of the discrete numeric function :

$0 \times 1, 1 \times 2, 2 \times 3, 3 \times 4, \ldots\ldots\ldots$

(b) Solve the recurrence relation $a_r - 2a_{r-1} + 2a_{r-2} - a_{r-3} = 0$, given that $a_0 = 2$, $a_1 = 1$ and $a_2 = 1$.

Or

8. (a) Determine the discrete numeric function corresponding to the generating function

$$A(z) = \frac{7z^2}{(1-2z)(1+3z)}.$$

(b) Let $4a_r + c_1 a_{r-1} + c_2 a_{r-2} = f(r), r \geq 2$ be a second order linear recurrence with constant coefficients. For some boundary conditions a_0 and a_1, the solution of the recurrence is $1 - 2r + 3 \cdot 2^r$. Determine a_0, a_1, c_1, c_2 and $f(r)$.

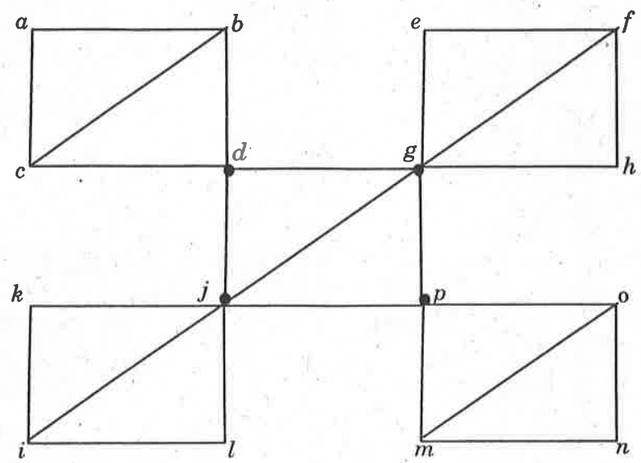
Module 5

9. (a) Show that in a connected planar linear graph with 6 vertices and 12 edges, each of the regions is bounded by 3 edges.

(b) Show that the sum of the in-degrees over all vertices is equal to the sum of the out-degrees over all vertices in any directed graph.

Or

10. Draw the different spanning trees in the following graph :



(5 × 20 = 100 marks)

F 3087 (Pages : 2) **Reg. No.....**

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering

MICROPROCESSOR SYSTEMS (R)

(Prior to 2010 Admissions—Old Scheme)

[Supplementary/Mercy Chance]

Time : Three Hours **Maximum : 100 Marks**

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. Give the flag register format of 8085 and explain each flag.
2. Explain with schematics, how separate address, data signals can be generated from 8085 common address/data lines.
3. Write and explain two methods to initialise stack pointer and FFFFH.
4. Is it possible to check the AC flag status of 8085 ? Explain.
5. Explain the various steps involved while executing CALL instruction with an example.
6. What is subroutine ? How is it useful ? Explain.
7. Distinguish between hardware and software interrupts.
8. Explain how 8085 responds to INTR interrupt.
9. List the important points which must be considered while interfacing memory devices in 8085.
10. Write a short note on serial communication supported by 8085.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. What is the maximum memory that 8085 can address ? Write neat block schematics, describe how the memory is organised and the chip select signals designed ?

Or

12. Describe the various address, data and control pins of 8085.

Turn over

13. Explain the operations of the following instructions and specify their addressing modes and show the machine cycles :—

(i) DAA ; (ii) XTHL ;

(iii) ADCr ; (iv) CMP M.

Or

14. Explain the operations performed by 8085 when the following instructions are expected :—

(i) SPHL ; (ii) RAR ;

(iii) DADrp ; (iv) XRA r.

Also show how the flags are affected in each case ?

15. Explain BCD to binary code conversion technique and write an ALP for the same.

Or

16. Draw and explain the :—

(i) Memory write and ;

(ii) I/O read cycle of 8085.

17. With the help of a neat flow chart, describe the polling routine in 8085.

Or

18. Draw the block diagram of 8259 and explain the function of each block.

19. An 8 KB ROM having a word length of 8 bits is to occupy the first 8 kB of the address space of an 8085. Two 2KB RAMs having word lengths of 4 bits each are to occupy 2KB starting from address 4000 H. Draw and design address decoding logic.

Or

20. With a block schematic of a DMA controller, explain the functions of each signal connected to it. Explain how the DMA controller effects the data transfer between memory and peripheral devices.

(5 × 12 = 60 marks)

F 3096 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering/Information Technology

SOLID STATE ELECTRONICS (R, T)

(Prior to 2010 Admissions—Old Scheme)

(Supplementary/Mercy Chance)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 marks.

1. Define d.c. load line and Q-point.
2. Draw the circuit and explain the emitter follower with capacitor load.
3. With neat circuit diagram, explain self biasing circuit for *n*-channel JFET.
4. Why a FET is known as unipolar device ? How do you compare this device with BJT ?
5. Find the frequency of the oscillations of transistorised Colpits oscillator having tank circuit parameters as C_1 = 150 pF, C_2 = 1.5 nF and L = 50 μH.
6. Explain how oscillations are initiated and later sustained in an oscillator circuit.
7. Draw the input and output waveforms of a low pass RC circuit to a pulse input.
8. What is commutating capacitor ? Explain its function in a multivibrator circuit.
9. What are the various types of IC voltage regulators ? Explain the operation of any *one* IC voltage regulator.
10. Explain the differences between a TRIAC and thyristor. Enlist the applications of TRIAC.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each question carries 12 marks.

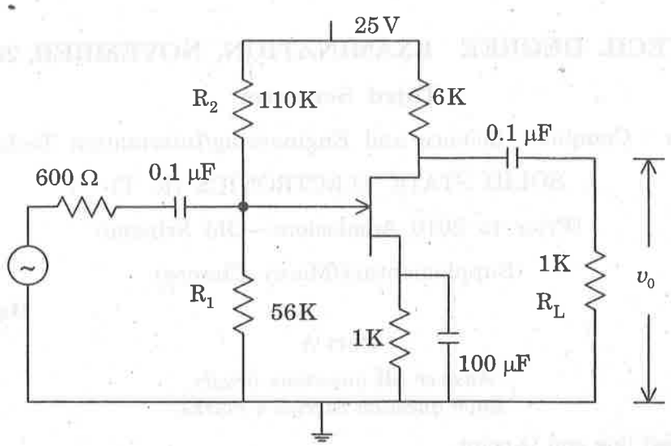
11. For the base bias circuit, (a) R_B = 150 kΩ and ; (b) R_B = 100 kΩ. Calculate I_B, I_C and V_{CE} if V_{CC} = 12 volt, R_C = 1.1 kΩ and β = 100. Also identify the operating regions of the transistor.

Or

12. Draw the Darlington pair circuit and derive its R_i, A_i, A_v and R_o.

Turn over

13. For the JFET amplifier circuit shown below :



g_m = 2.5 mS, r_d = 200 $k\Omega$, C_{gs} = 12 pF, C_{gd} = 2pF $R_1//R_2$ = 0.1 M, $C_W + C_L$ = 10 pF

(i) Draw the linear circuit for midfrequencies and calculate the midfrequency gain.

(ii) Determine the low frequency cut-offs caused by the input and output circuits. Which one of these is the low frequency cut-off of the complete frequency response ?

(iii) Determine the upper cut-offs caused by input and output circuits. Which one of these is the high frequency cut-off of the complete frequency response ?

Or

14. With neat diagrams explain the construction of an enhancement type p-channel MOSFET. Draw and explain its static characteristics. How is the threshold voltage of the MOS transistor adjusted ?

15. In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 KHz to 2050 KHz. Calculate the range over which the capacitor is to be varied. Draw the circuit and explain how sine waves are produced in it ?

Or

16. With neat circuit diagram, explain how sine was are produced in a transistor Wienbridge oscillator. Compare and contrast it with RC phase shift oscillator.

17. Draw the circuit diagram of astable multivibrator using transistors. Prove that the expression for the period of oscillation is 2T log 2, taking into account the $V_{CE_{sat}}$, $V_{BE_{sat}}$ and the cut-in voltage of the transistor.

Or

18. With a neat circuit diagram, describe the working of a transistorised Bootstrap time base generator. Explain clearly, the quiescent conditions, the formation of sweep, the retrace interval and the recovery process.

19. Explain the voltage adjustment provided by LM 317. Explain a circuit using LM 317 to obtain V_0 from 5V to 12 V, I_0 = 1 Amp. Design your circuit diagram.

Or

20. With a neat constructional diagram, explain the working of SCR. Explain its VI characteristics and describe how controlled rectification can be achieved ?

(5 × 12 = 60 marks)

F 3113 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch—Computer Science and Engineering/Information Technology

HUMANITIES (R, T)

(Prior to 2010 Admissions—Old Scheme)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Answer Part A and Part B in **separate** *answer books.*
Part A and Part B carry 50 *marks each.*
All full questions carry equal marks.

Part A (Principles of Management)

Answer any **one** *full question from each module.*

MODULE 1

1. (a) Explain the following functions of management :—

(i) planning ; (ii) directing ; and

(iii) staffing.

Or

(b) Explain the following :—

(i) functional organisation ;

(ii) matrix organisation ; and

(iii) Committee organisation.

Give their merits and demerits.

MODULE 2

2. (a) Explain clearly the tools and techniques used in total quality management.

Or

(b) What is the necessity of ISO 9000 certification ? Explain the main features of ISO 9000 certification process.

(50 marks)

Turn over

Part B (Engineering Economics)

Answer any **one** *full question from each module.*

MODULE 3

3 (a) (i) Describe the quantitative controls which the RBI adopts to regulate money supply.

(ii) How does RBI control credit ?

Or

(b) (i) **Explain how the commercial banks reconcile the conflicting aims of liquidity and profitability in their operations.**

(ii) **Examine the case for and against the use of the method of variable reserve ratios for the control of bank credit.**

MODULE 4

4. (a) (i) Discuss the important features of new industrial policy of the Government of India.

(ii) Distinguish between large scale and small scale industries, bringing out their significances.

Or

(b) Critically examine the industrial growth in India since independence. Suggest your views for future development.

MODULE 5

5. (a) (i) Explain the social and economic objectives of taxation.

(ii) Bring out the money burden and real burden of public debt both internal and external.

Or

(b) (i) What is black money ? What are its consequences ? How it can be controlled ?

(ii) Discuss the major purposes for which public debt is incurred.

(50 marks)

F 3127 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Common to all Branches

EN 010 302—ECONOMICS AND COMMUNICATION SKILLS (AI, AN, AU, CE, CH, CS, EC, EE, EI, IC, IT, ME, MT, PE, PO, ST)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 3 *marks.*

1. What are the objectives of credit control ?
2. What is WTO ? What are its objectives ?
3. State the merits of indirect taxes.
4. List the different types of inflation.
5. Distinguish between free trade and protection.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. What is meant by credit creation ? What are the tendencies behind credit creation ?
7. Render your comments on the disinvestment of public sector undertakings.
8. What are the differences between a tax on income and tax on a commodity ? Why is a tax on income preferred in modern times ?
9. What are the major methods of measuring national income ? Explain.
10. State and explain the various items included in the balance of payments of a country.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. What are the main functions of banks ? Explain the role played by Commercial banks in the economic development of a country.

Or

12. "Stock market can be regarded as an economic barometer." Critically examine this statement in the context of Indian economy.

13. What are the measures taken by Indian Government in the case of Globalisation, Liberalisation and Privatisation. Explain their impacts on Indian economy.

Or

14. Discuss the past, present and future prospects of Information Technology industries on Indian economy.

15. (a) Distinguish between Forward and Backward shifting of tax. Explain the impact and incidence of tax.

(7 marks)

(b) Explain progressive, proportional and regressive taxes with suitable examples. (5 marks)

Or

16. (a) Explain the important problems associated with deficit financing in Indian Economy.

(7 marks)

(b) Define tax evasion. Explain the reasons for the same in India. (5 marks)

17. (a) Define National Income. What are its concepts ? Explain the difficulties arising in the calculation of National Income.

(7 marks)

(b) Explain the significance of national income statistics. (5 marks)

Or

18. Describe the different types of inflation and their causes. What are the steps taken by the Government to control the same ? Explain.

19. What are the different types of disequilibrium in BOP ? Explain the causes for and the methods of correcting disequilibrium in BOP.

Or

20. What are the main causes of India's adverse balance of payments ? Explain the measures that have been adopted to correct the adverse balance of payments. Critically examine India's trade policy.

[5 × 12 = 60 marks]

F 3141 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering

CS 010 304—COMPUTER ORGANISATION (CS)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 3 *marks.*

1. Suggest any one technique and briefly explain the same, to speed up the multiplication operation.
2. Write a note on floating point number representation.
3. What is microinstruction ? Write the format of microinstruction.
4. State two techniques to reduce cache miss penalty.
5. Differentiate between logical address and physical address.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Give steps for performing non-restoring division.
7. Describe how floating point multiplication can be carried out in a computer.
8. Explain micro-instruction sequencing with next address field.
9. With a neat block diagram, show how the performance of memory can be improved in interleaved organization of multiple memory modules.
10. Explain how a virtual address is mapped to physical address using page table.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Multiply the following pair of signed 2's complement numbers using the Booth algorithm :

A = 01101011 (Multiplicand)

B = 10110010 (Multiplier)

Or

12. (a) Illustrate with an example the algorithm for restoring division. (6 marks)

(b) With necessary diagrams, describe the working of a 4-bit carry look-ahead adder. (6 marks)

13. With necessary flow-charts, explain how floating point addition and multiplication are performed in a computer.

Or

14. Construct a 32-bit ALU from 1 bit ALU and explain how it performs various logical operations.

15. Design a microprogrammed and also hardwired control unit for bit pair multiplication scheme. Give the data path and control path with binary listing of the microprogram.

Or

16. (a) What are the different schemes followed in optimizing the control memory in microprogram control ?

(6 marks)

(b) Compare hardwired and microprogrammed approaches in the design of control units.

(6 marks)

17. Organize the subfields of MAR to realize a block set associately mapped Cache-Main storage hierarchical memory with MS capacity of 16K pages of 16 word each and cache capacity of 256 pages divided into sets, each set having 8 pages.

Or

18. What are the placement policies and replacement policies in memory hierarchy ? Explain the common placement and replacement policies present in memory allocation.

19. What is memory paging ? Explain the paging registers, page directory and page table with neat diagrams.

Or

20. (a) Explain how the translation buffers speed up logical address generation. (7 marks)

(b) What is TLB miss ? How it is handled ? (5 marks)

[5 × 12 = 60 marks]

F 3151 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering/Information Technology

CS 010 305/IT 010 304—SWITCHING THEORY AND LOGIC DESIGN (CS, IT)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 3 *marks.*

1. Find the value of x in the following :—

   (a) $(847)_{10} = (x)_{16}$.

   (b) $(10110101)_2 = (x)_8$.

   (c) $(A3BH)_{16} = (2619)_{10}$.

2. Draw a half adder circuit using NOR gates only.

3. Write down the truth table and characteristic equation of SR flip-flop.

4. How are shift-left or shift-right transfer registers built ?

5. What do you mean by hazard-free asynchronous sequential circuits ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Convert the following into cannonical forms :

   (a) $\overline{A}B + AB\overline{C}D + \overline{B}\,\overline{C}$.

   (b) $(\overline{A} + C)(A + \overline{B})(B + C)$.

7. Using full-adder blocks, represent the following 4-bit addition ;

   1111 + 1011.

Turn over

8. Distinguish between truth table and excitation table, taking JK flip-flop as example. How the excitation table can be derived from the truth table ?
9. Construct a Johnson counter for ten timing signals ?
10. What is fault tolerance ? Explain different fault tolerance techniques.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Design the circuit for a 2 bit BCD-to- binary coverter, with the help of the function tables.

Or

12. Reduce using Quine McCluskey method $S = \sum(1, 2, 4, 5, 6, 8, 9, 12) + d(3, 10, 13, 15)$. Draw reduced prime implicants table and the minimal reduced circuit.
13. (a) What is a full subtractor ? Design the same using K-maps and draw the minimal circuit.

(6 marks)

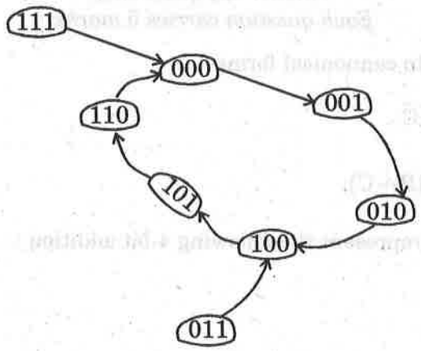
(b) With a neat block diagram, explain a 4 bit carry look-ahead adder. (6 marks)

Or

14. Design a gray-to-binary code converter using 4 : 1 MUX. Draw the circuit diagram and explain.
15. A network produces a '1' output if and only if the current input and the previous three inputs correspond to either of the sequences 0110 or 1001. The output '1' is to occur at the time of the fourth input of the recognised sequence. Outputs of zero are to be produced at all other time. Construct the state diagram.

Or

16. Design a sequential machine with one input and one output line such that the output becomes '1' when the input receives a sequence 101. Overlapping of sequence is allowed. Use D-flip-flops.
17. Design a synchronous counter using JK flip-flop for the state diagram given in figure.



Or

18. (a) With neat diagrams and waveforms, explain a 4 bit shift register with left/right shift control and with parallel load control.

(6 marks)

(b) Design a mod-77 synchronous counter by cascading two 4-bit binary counters. (6 marks)

19. (a) With an example, explain one method of designing a hazard-free network. (5 marks)

(b) Design the following network, which is free of static and dynamic hazards. Design the circuit using NAND gates only $F(a, b, c, d) = \sum m(1, 5, 7, 14, 15)$.

(7 marks)

Or

20. (a) Draw the internal circuit diagram of a CMOS NAND gate and explain its working.

(7 marks)

(b) Compare the performance parameters of TTL, CMOS and ECL families. (5 marks)

(5 × 12 = 60 marks)

(b) Explain the working of the high pass filter as a differentiator. (5 marks)

Or

20. Draw the internal functional block diagram of 555 timer. Show how it can be used to generate a time delay pulse of 0.6 m sec. Explain the working with related waveforms.

(5 × 12 = 60 marks)

F 3160 (Pages : 4) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2014

Third Semester

Branch : Computer Science and Engineering

CS 010 306—ELECTRONIC DEVICES AND CIRCUITS (CS)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *question briefly.*

Each question carries 3 *marks.*

1. Write the values of maximum efficiency of rectification in the *three* rectifier circuit.
2. Draw the *h*-parameter model of CE transistor.
3. Draw the circuit of voltage follower using op-amp.
4. Which type of oscillator is preferred when high stability of frequency is required ? Why ?
5. What are the differences between astable and monostable multivibrators ? Explain.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. Using 7809, draw a voltage regulator circuit. Specify the range of input that can be applied ?
7. Sketch the input and output characteristics of an *npn* transistor of CE configuration.
8. Draw the block diagram of the internal blocks in an operational amplifier and explain the functions of each block.
9. State and explain any *five* advantages of negative feedback in amplifiers.
10. Plot the step response of low pass RC circuit for : (i) Very low (ii) Medium (iii) High time constants.

(5 × 5 = 25 marks)

Part C

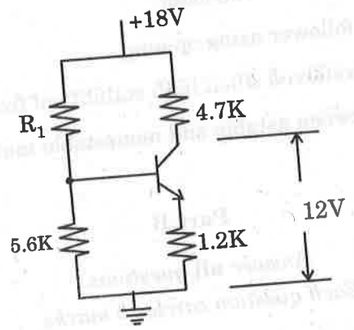
Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Draw the complete circuit diagram of a centre-tapped rectifier using LC filter and explain its working with necessary waveforms.

Or

12. With a circuit diagram, explain how a series voltage regulator provides regulation against (a) line voltage variations ; (b) load current changes.

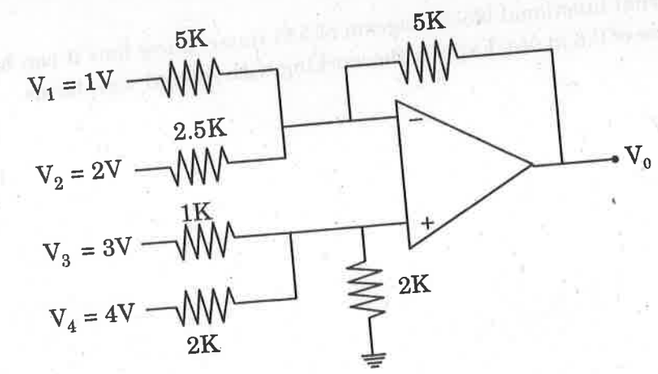
13. For the circuit shown in fig. 1 below using silicon transistor with V_{BE}= 0.7 volt, find (a) collector current ; (b) Emitter and base voltages with respect to ground ; (c) value of R_1 ; and (d) Plot the d.c. load line and mark the Q-point.



Or

14. In a fixed bias circuit, the coordinates of the Q point which is located at the centre of the d.c. load line are V_{CE} = 5 Volt and I_C = 2mA. calculate V_{CC}, R_C and R_B. Assume a silicon transistor with β =100.

15. (a) For the op-amp circuit shown below, find the output voltage V_0.



(7 marks)

(b) Draw and explain ideal voltage transfer curve of an op-amp. (5 marks)

Or

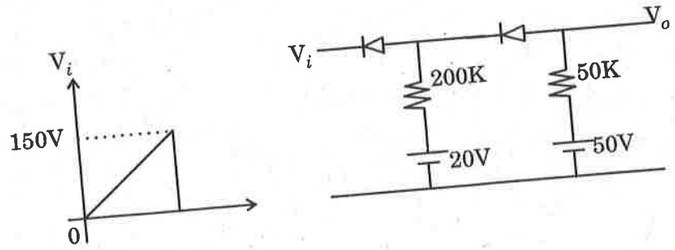
16. Give the circuit of a difference amplifier in which the gain can be varied by a single potentiometer control. Hence derive the expression for its gain.

17. Draw a circuit of BJT amplifier having negative current series feedback. Analyse the circuit to derive its gain, input resistance and output resistance with feedback.

Or

18. With a neat circuit diagram, explain the working of RC phase shift oscillator using op-amp. Derive the expression for the oscillator frequency.

19. (a) Find the output V_o for the circuit shown below Assume silicon diode having Vr = 0.7 volt.



(7 marks)