Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

THIRD SEMESTER B.TECH DEGREE EXAMINATION(S), MAY 2019

Course Code: IT201

Course Name: DIGITAL SYSTEM DESIGN

Max. Marks: 100 Duration: 3 Hours

PART A

Answer any two full questions, each carries 15 marks.

Marks

1 a) Convert $(76.75)_{10}$ to binary, octal and hexadecimal. (3)

b) Perform subtraction using 2's complement of the subtrahend of **1100.101 – 101.1011** (4)

c) Determine the base of the numbers in the operation; $\frac{58}{4} = 15$ (3)

d) Represent the unsigned decimal numbers **572.36** and **382.71** in BCD. Show the necessary steps to form their sum. (5)

2 a) Prove that $A+\bar{A}B = A + B$ using Boolean postulates. (5)

b) Find the complement of the Boolean function $F = \bar{A} + AB\bar{C}$.And prove that $F + \bar{F} = 1$and $F.\bar{F} = 0$. (5)

c) Simplify the Boolean expression to minimum number of literals.

$$F = \bar{B}\bar{C} + A\bar{B} + AB\bar{C} + AB\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}CD$$ (5)

3 a) Represent (+59) and (-31) as signed binary numbers using 2's complement representation enough digits to accommodate the numbers. Perform the addition of these signed binary numbers. (5)

b) Minimise the following Boolean function using Quine – McClusky method

$$F(A,B,C,D) = \Sigma_m(2,4,5,10,12,13) + \Sigma_d(0,3,8,11,15)$$ (10)

PART B

Answer any two full questions, each carries 15 marks.

4 a) Explain the design procedure of a combination circuit (5)

b) Design a look ahead carry generator to add two four-bit binary data input (10)

5 a) Give the characteristics equations for D, JK and T flip-flops. (3)

b) Explain the state reduction in the sequential circuits using an example. (12)

6 a) A communication system uses four bits to transfer information. The system uses even-parity to identify the error during transmission and the LSB bit represent the parity bit. Design a parity checker for this system. (4)

b) Design a 4-to-2 line priority encoder. (4)

c) What are pulse-triggering and edge-triggering? Draw the circuit diagram of D-latch and D- flip-flop. Using the timing diagram of D-latch and D- flip-flop, show the difference between pulse-triggering and edge-triggering. (7)

PART C

Answer any two full questions, each carries20 marks.

7 a) Implement a serial adder using a shift register. (6)

b) Design and implement a BCD ripple counter. Show the complete timing diagram for 12 clock pulse. (14)

8 a) Write the HDL gate-level behaviour description of a four-to-one line multiplexer. (6)

b) Design and implement a combinational circuit using a ROM that accepts a three-bit binary number as input and outputs a binary number equal to square of the input number. (10)

c) What are the steps that must be taken during write and read operations of a RAM? (4)

9 a) Design and construct a 4-bit ring counter with only one flip-flop is clear at any particular time and all other flip-flops are set. Give its timing diagram. (10)

b) Write the HDL gate-level dataflow description of a four bit adder. (6)

c) Using Booth algorithm, perform multiplication of (+14) and (-7). (4)

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