F 4881 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication Engineering

EC 010 503 – DIGITAL SYSTEM DESIGN (EC)

(New Scheme – 2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 3 *marks.*

1. Write the verilog HDL program for a full adder.
2. What is PAL, PLA?
3. What is meant by metastability?
4. Describe an ASM chart.
5. What do you mean by FSM?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. Describe different datatypes used in VHDL.
7. Explain how a decoder can be used for implementing a Boolean function.
8. Describe (a) State diagram ; (b) State table ; and (c) State assignment.
9. How an ASM chart helps in explaining a digital circuit.
10. Explain the principle of workong of a Barrel shifter.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*

Each question carries 12 *marks.*

11. Describe the different types of modelling used in VHDL.

Or

12. Design a binary to gray code converter.

Turn over

13. Implement the given function using a multiplexer $f(x, y, z) = \Sigma m\ (0, 2, 3)$.

Or

14. Explain the Quine-Mc Cluskey algorithm.

15. Design a BCD adder circuit.

Or

16. Design a sequence detector circuit for detecting the sequence "1010", overlapping of bits in the sequence is allowed.

17. Explain the different steps involved in the design of a clocked sequential circuit.

Or

18. Draw an ASM chart for a circuit which generates parity bit.

19. Write notes on : (a) FSM ; (b) Shift register.

Or

20. Design and write verilog HDL for a binary multiplier.

(5 × 12 = 60 marks)

F 4895 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication Engineering

EC 010 504 – ELECTRICAL DRIVES AND CONTROL (EC)

(New Scheme – 2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 3 *marks.*

1. List out the different methods of speed control of DC motor.
2. Draw the phasor diagram of a transformer on load.
3. Draw the V-I characteristics of an IGBT during turn ON and turn OFF.
4. List out some of the applications of SMPS.
5. List out the speed control methods of three-phase induction motor.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. Explain the procedure for Swinburn's test with the help of a neat diagram.
7. Describe the method of obtaining regulation by e.m.f. and m.m.f. methods.
8. Describe briefly the constructional details of MOSFET.
9. Draw the block schematic of UPS and explain the principle of operation.
10. Discuss the rotor resistance control of induction motor drives mentioning its advantages.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. Explain in detail the procedure for obtaining load characteristics of a DC shunt generator.

Or

12. Explain the speed torque characteristics of DC shunt, series and compound motors.

Turn over

13. (a) Describe the principle of operation of three-phase induction motors with the help of neat figure.

    (b) Explain about the production of rotating magnetic field using three-phase supply.

(6 + 6 = 12 marks)

Or

14. (a) Derive the e.m.f. equation of an alternator.

    (b) What are the losses in an alternator? Explain briefly about each of them.

(6 + 6 = 12 marks)

15. Explain about the constructional details of TRIAC with the help of neat figure.

Or

16. Discuss about the different types of switching device protection.

17. Draw the power circuit of a single-phase current source inverter and explain the principle of operation with the relevant waveforms.

Or

18. Draw the power circuit of a single-phase fully controlled converter with RL load and explain the principle of operation with necessary graphs. Also derive the output voltage equation.

19. Draw the circuit of a single quadrant chopper fed separately excited DC motor drive and explain its output voltage control methods.

Or

20. Draw and explain the block diagram of variable frequency PWM inverter fed three-phase induction motor drive.

[5 × 12 = 60 marks]

F 4923

(Pages : 2)

Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication Engineering

EC 010 506 – MICROPROCESSORS AND APPLICATIONS (EC)

(New Scheme – 2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours

Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 3 *marks.*

1. What are the functions of a microprocessor? Explain in detail.
2. Convert the binary number stored at the location 2003 H into decimal form and display the decimal number on the address field of the microprocessor kit.
3. What is tri state logic? Explain with its diagram.
4. Explain the instructions associated with memory mapped I/O.
5. Explain any *three* addressing modes of Intel 8086 in detail.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. Discuss the differences between microprocessors and microcontrollers.
7. Write an ALP to find smallest number in a given data array. Explain the steps.
8. Explain the significance and types of interrupts in detail.
9. Explain the peripheral interface side of 8257 with a diagram.
10. Explain the segment registers of Intel 8086 in detail.

(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. (i) Explain the architecture of a microprocessor with a neat diagram.

(ii) Explain the concept and significance of memory interfacing in detail.

Or

12. (i) Explain the 8085 instruction set in detail.

(ii) Explain the need for timing diagram with an example.

13. (i) Explain stack and subroutine with examples.

(ii) Write an ALP to multiply two 8-bit numbers stores at 2000 H and 2001 H and display the result in the address field of the microprocessor kit.

Or

14. (i) Write an ALP to arrange numbers in a data array in ascending orders.

(ii) Explain the programs in looping and counting with examples.

15. (i) Explain the steps to interface input and output devices.

(ii) Give an account on "Interfacing ADC and DAC".

Or

16. (i) Explain the interfacing circuit for 8-bit output port with a diagram.

(ii) Explain the different ways of organizing I/O devices.

17. Explain the pin diagram of 8257 DMA controller in detail.

Or

18. (i) Explain the following in detail : (a) DMA channels ; (b) Slave mode operation.

(ii) Give an account on "memory mapped I/O and I/O mapped I/O schemes".

19. (i) Explain the difference between 8-bit and 16-bit microprocessor.

(ii) Explain the interrupts of intel 8086 with examples.

Or

20. (i) Explain the block diagram of intel 8086 in detail.

(ii) Write a technical note on "Even and odd memory banks".

(5 × 12 = 60 marks)

F 4856 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication/Electronics and Instrumentation Engineering

MICROPROCESSORS AND MICROCONTROLLERS (LS)

(Old Scheme—Supplementary/Mercy Chance)

[Prior to 2010 Admissions]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Explain the tristate bus concept and its uses.
2. How the address and data lines are demultiplexed in 8085 ?
3. List the special function registers of 8051.
4. Draw and explain the port 0 circuit, giving its important features.
5. Draw the internal RAM memory map of 8051.
6. What is PSW ? Explain its parts.
7. Name the interrupt sources of 8051 and specify their vector address.
8. Explain the single step operation and its uses.
9. How the TMOD registers are used to configure the timers/counters in 8051 ?
10. Explain the ONCE mode.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. What is the maximum memory that can be addressed by 8085 ? With neat block schematics describe how the memory is organized and the chip select signals designed.

Or

12. With a neat timing diagram, explain the opcode fetch operation from the memory, sketching IO/$\overline{M}$, S_0, S_1, A_0 to A_{15} and $\overline{RD}$ signals, with reference to the clock signals.

Turn over

13. With suitable diagrams, explain the function of the PORTS of 8051.

Or

14. (a) Describe the functions of PSEN, EA, XTAL1 and XTAL2 pins of 8051.

(b) Explain the flash programming techniques in 8051.

15. Describe how memory space is divided into many groups, with the help of neat sketches.

Or

16. (a) Compare data memory and program memory of 8051.

(b) Explain Boolean and program branching instruction set of 8051.

17. Explain various interrupts and interrupt handling in 8051.

Or

18. With relevant details, explain the interfacing of 8051 to external memory.

19. Explain how serial communication is implemented in 8051. Explain the modes 0, 1, 2, 3.

Or

20. Write a ALP to generate square wave of approximate frequency 500 Hz with a subroutine to provide a delay of approximately 30 μs using timer 0. Assume crystal frequency of 11.0592 MHz.

(5 × 12 = 60 marks)

F 4848 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication/Electronics and Instrumentation/Applied Electronics and Instrumentation Engineering

LINEAR INTEGRATED CIRCUITS (LAS)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. List six characteristics of an ideal op-amp.
2. Define slew rate. What causes the slew rate ?
3. What is offset minimising resistor R_{comp} ?
4. Show with the help of circuit diagram an op-amp used as (a) scale changer ; (b) phase shifter.
5. What is VCO ? Give two applications that require a VCO.
6. What is roll-off rate of a first order filter ?
7. How we do get a notch filter from a bandpass filter ?
8. What is a voltage regulator ? List four different types of voltage regulation.
9. Explain the current limiting feature of 723 regulator.
10. Explain the protections used in 78XX.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Explain differential mode gain, common mode gain and common mode rejection ratio of op-amps. What are the methods to improve CMRR ?

Or

12. Explain the op-amp parameters and methods of determining the op-amp parameters with necessary circuits and derivations.

Turn over

13. Explain adder, subtractor, integrator and differentiator with op-amps and derive the necessary output voltage equation and relevant output waveforms.

Or

14. Explain the principle of operation of a voltage to current converter which uses a grounded load. Derive expression for its output.

15. With a neat circuit diagram, explain a RC phase shift oscillator using op-amp. Derive the expression for frequency of oscillations and conditions for sustained oscillations.

Or

16. With neat circuit diagram and relevant waveforms explain the working of a simple op-amp square wave generator. Derive the expression for frequency of oscillations.

17. Explain with necessary diagrams, a 555 timer can operate in (i) Astable mode ; and (ii) Monostable mode.

Or

18. Differentiate between First order and Second order LPF and HPF filters. Derive the relevant equations.

19. Explain the FSK demodulation with neat circuit diagram in which 565 PLL is used as an FSK demodulator.

Or

20. Explain LM 380 circuit and also explain how it can be used as an audio power amplifier.

(5 × 12 = 60 marks)

F 4817 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication Engineering

POWER ELECTRONICS (LA)

(Old Scheme – Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 4 *marks.*

1. Enumerate the different turn on methods of thyristor.
2. Discuss the conditions which are to be satisfied for turning on an SCR with gate signal.
3. Discuss about the advantages of freewheeling diode.
4. Draw the voltage and current waveform of a fully controlled rectifier with RL load.
5. Discuss the principle of cycloconverter.
6. What do you mean by integral cycle control?
7. Draw the circuit diagram of a type E chopper.
8. Discuss the disadvantages of frequency modulation when compared to pulse width modulation scheme in case of chopper.
9. Enumerate the applications of CSI.
10. What are the two main types of inverters? Distinguish between them.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. Discuss in detail about the design of Snubber circuit and various protection of thyristors.

Or

12. Explain in detail about the static V–I characteristics and switching characteristics of GTO.

Turn over

13. Discuss the effect of source inductance on the performance of a single-phase full converter indicating clearly the condition of various thyristors during one cycle. Derive expressions for its output voltage.

Or

14. Write relevant waveforms and circuit diagram, explain the operation of single-phase diode rectifier with RL load and freewheeling diode.

15. Derive an expression for the output voltage equation for a cycloconverter. Enumerate some of the industrial applications of a cycloconverter.

Or

16. (a) A single-phase voltage controller has input voltage of 230 V, 50 Hz and a load of R = 15 Ω. For 6 cycles on and 4 cycles off, determine : (a) r.m.s. output voltage ; (b) Input power factor ; (c) Average and r.m.s. thyristor currents.

    (b) Explain in detail about the integral cycle control of AC voltage controller with suitable waveforms.

(6 + 6 = 12 marks)

17. With necessary waveforms, explain the working of a current commutated chopper.

Or

18. (a) For type A chopper, d.c. source voltage = 230 V, load resistance = 10 Ω. Take a voltage drop of 2 V across chopper when it is on. For a duty cycle of 0.4, calculate (a) Average and r.m.s. values of output voltage ; and (b) Chopper efficiency.

    (b) A step-up chopper has input voltage of 220 V and output voltage of 660 V. If the non-conducting time of thyristor chopper is 100 μs, compute the pulse width of output voltage. In case pulse width is halved for constant frequency operation, find the new output voltage.

(6 + 6 = 12 marks)

19. With relevant waveforms, explain the operation of 120 mode, 3-phase voltage source inverter.

Or

20. Explain the operation of single-phase voltage source inverter with R and RL load with suitable waveforms.

[5 × 12 = 60 marks]

F 4869 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2015

Fifth Semester

Branch : Electronics and Communication Engineering

EC 010 502—CONTROL SYSTEMS (EC)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Graph sheets and Semilog sheets are to be supplied.

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. What are analogous systems ? Why electrical analogy is preferred compared to others, for studying non-electrical systems ?
2. Define steady-state error in control systems. What are its causes ? How we can calculate it ?
3. What are the different compensation methods ? What all factors are to be considered while choosing the compensation method for a given system ?
4. What are the advantages of Bode plot compared to traditional methods ?
5. Define state, state model and state transition matrix of a dynamic system.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Define Transfer function. What are its merits and limitations ?
7. What are test signals ? Write the name of any four test signals and give its graphical representation and Laplace Transforms.
8. Define Root Locus of a system. What are its Basic properties ? How stability can be determined using Root Locus plot ?
9. What is Nyquist stability criterion ? State principle of arguement theorem.
10. What are the conditions to be followed while using state space modelling of a system ?

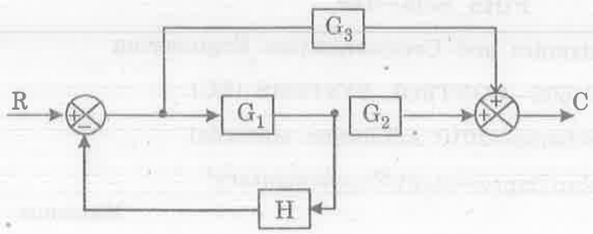
(5 × 5 = 25 marks)

Turn over

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. (i)



Reduce the Block diagram and obtain $\frac{C}{R}$.

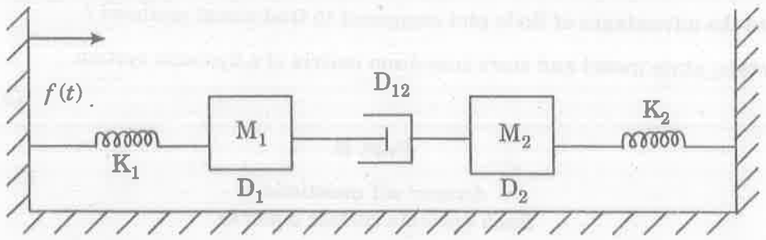
(8 marks)

(ii) List down the transient response characteristics of a control system for a unit stap input and give its graphical representation.

(4 marks)

Or

12. Write the differential equation and obtain the force voltage analogous network for the system shown below :



13. A unity Feedback system is characterized by the open loop transfer function $G(s) = \frac{1}{s(0.5s+1)(0.2s+1)}$.

Determine the steady-state error for unit step input, unit Ramp input and parabolic input. Also determine the daming ratio and natural frequency of dominant Roots.

Or

14. The open loop transfer function of a servo system is given by $G(s)H(s) = \frac{400}{s(1+0.3s)}$. Evaluate the Dynamic Error series of the system. Determine the steady-state error from the error series for an input $r(t) = 1 + 2t + t^2$ and verify the same using static error co-efficients.

15. A units feedback control system has an open loop Transfer function $G(s) = \frac{K}{s(s^2+4s+13)}$. Sketch the Root locus and discuss about its stability.

Or

16. Draw Lag and Lead Compensating networks and obtain its Transfer Function. Sketch their Bode plots. Discuss the situations where these compensators are to be preferred. What are the limitations of lead compensators ?

17. For the given open loop Transfer Function $G(s)H(s) = \frac{5(1+2s)}{(1+4s)(1+0.25s)}$, draw the Bode plot and determine the stability of the system.

Or

18. (i) State the 'Centre' and 'Radius of constant M circle'.
(ii) Define Nyquist stability criterion.
(iii) Mention the advantages of Nichol's chart.
(iv) Define Gain Margin and Phase Margin.

(4 × 3 = 12 marks)

19. Compute the state transition matrix for the system with $A = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix}$ using Laplace transform techniques.

Or

20. (i) Diagonalise the matrix :

$$A = \begin{bmatrix} 0 & 1 & 0 \\ 3 & 0 & 2 \\ -12 & -7 & -6 \end{bmatrix}.$$

(8 + 4 = 12 marks)

(ii) Define Eigen values and Eigen vectors.

[5 × 12 = 60 marks]