G 5179

(Pages : 2)

Reg. No........................

Name........................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch—ECE/Applied Electronics and Instrumentation/
Electronics and Instrumentation Engineering

COMPUTER NETWORKS (LAS)

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

*Answer **all** questions.*

Part A

Each question carries 4 marks.

1. What is a Distributed system ?

2. Discuss the different LAN topologies.

3. What is a shared memory ?

4. Explain the concept of Polling.

5. Define confidentiality.

6. Write briefly on WAP technology.

7. Explain an ATM cell.

8. What is a virtual circuit ?

9. Explain Remote procedure call.

10. Discuss the functions of Transport layer.

$(10 \times 4 = 40 \text{ marks})$

Part B

Each question carries 12 marks.

11. Explain TCP/IP reference model. Discuss the functions of each layer.

Or

12. Explain the different media used in guided transmission.

(12 marks)

13. (a) Explain the need for Data link layer.

(6 marks)

(b) Explain the stop and wait and sliding window protocol.

(6 marks)

Or

Turn over

14. Explain :

    (a) Congestion control.

    (b) Routing.

15. Explain CSMA|CD mechanism.   (12 marks)

                                              (12 marks)

Or

16. (a) Explain the design issues involved in the Transport layer.

                                              (6 marks)

    (b) Write a note on Crash Recovery.

                                              (6 marks)

17. (a) Explain the principles of Cryptography.

                                              (6 marks)

    (b) Write briefly on presentation layer in ARPANET.

                                              (6 marks)

Or

18. (a) Discuss the design issues of session layer.

        (6 marks)

    (b) Write briefly on Network security.

                                              (6 marks)

19. Explain the ATM protocol architecture.

                                              (12 marks)

Or

20. (a) Explain File Transfer protocol.

                                              (6 marks)

    (b) Discuss the basic principles of SONET.

                                              (6 marks)

                                          [5 × 12 = 60 marks]

G 5187 (Pages : 2) Reg. No...................................

Name...................................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : Electronics and Communication Engineering

ADVANCED COMMUNICATION SYSTEMS (L)

(Regular/Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer all questions.
Each question carries 4 marks.

1. Define transmission path. Give its representation.
2. What is tracking ? Explain.
3. Explain the role of multiple access techniques in communication systems.
4. What is packet switching ? Give its advantages over circuit switching.
5. What is cell splitting ? Name and explain different factors that affect cell splitting.
6. Explain the basic principle of blue tooth technology.
7. Explain how the third generation cellular network changes from second generation.
8. List different applications of GPS.
9. Explain the concept of jamming. Why is it employed ?
10. What is remote sensing ? List its applications.

(10 × 4 = 40 marks)

Part B

Answer all questions.
Each question carries 12 marks.

11. (a) What are geostationary satellite ? Explain the following terms of geosynchronous satellites.

(2 marks)

    (i) Orbital velocity.

    (ii) Round trip time delay.

    (iii) Advantages and disadvantages.

(3 × 2 = 6 marks)

  (b) Write short notes on INSAT.

(4 marks)

Or

12. (a) With block diagram, explain a satellite uplink model. (6 marks)

    (b) Define the following :

        (i) Equivalent noise–temperature.

        (ii) S/N ratio.

                                                                  $(2 \times 3 = 6$ marks)

13. Explain the working principle of FSS satellite communication system. (12 marks)

Or

14. Describe the following :

    (a) CDMA.

    (b) Packet satellite network.

                                                       $(2 \times 6 = 12$ marks)

15. (a) What is frequency reuse ? Explain how it is employed in a cellular network. (6 marks)

    (b) Explain different hand off strategies in practical hand off implementation. (6 marks)

Or

16. Describe the following :

    (a) Co-channel interference. (6 marks)

    (b) Adjacent channel interference. (6 marks)

17. (a) Name different components of a cellular telephone system and briefly explain about each one. (6 marks)

    (b) What is PCS and PCN ? Explain briefly. (6 marks)

Or

18. (a) Describe the concept of digital cellular telephony. (6 marks)

    (b) With block diagram explain the architecture of a GSM system. (6 marks)

19. (a) Illustrate the concept and principle of spread spectrum techniques. (4 marks)

    (b) With block diagram, explain the working principle of Time hopping modulator and receiver. (8 marks)

Or

20. (a) With diagram, explain the generation of 15-bit PN sequence. (8 marks)

    (b) Explain the following in connection with the above circuit.

        (i) Maximal length sequence. (1 mark)

        (ii) Clustering in a PN sequence. (1 mark)

        (iii) Balancing and auto correlation property. (2 marks)

                                                  $[5 \times 12 = 60$ marks]

G 5199   (Pages : 2)   Reg. No...............................

Name....................................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : E.C.E./Applied Electronics and Instrumentation/
Electronics and Instrumentation Engineering

ADVANCED MICROPROCESSORS (LAS)

(Regular/Supplementary)

Time : Three Hours   Maximum : 100 Marks

Answer **all** *questions.*

Part A

Each question carries 4 marks.

1. Discuss the minimum and maximum mode of operation of 8086 processor.

2. Explain the features of 8087 Math coprocessor.

3. With examples, explain direct program memory addressing.

4. Explain how Stack Addressing is done in 8086 processor.

5. What is meant by real mode of operation? Explain.

6. How memory address is calculated in protected mode in 80286?

7. What is meant by Virtual Memory? Explain with reference to 80386 processor.

8. What are Call Gates? Explain briefly.

9. Discuss the U-V pipeline in pentium processor.

10. Discuss briefly on the Integrated Coprocessor in pentium.

(10 × 4 = 40 marks)

Part B

Each question carries 12 marks.

11. (a) Explain the Interrupts and Interrupt applications in 8086 processor.

     (b) How physical address is formulated in 8086 processor?

Or

12. Discuss with neat block diagram the pipelined architecture of 8086 processor.

Turn over

13. Explain with examples the following data addressing modes of 8086 processor :—

(a) Immediate addressing.

(b) Direct addressing.

(c) Index addressing.

(d) Indirect addressing.

Or

14. (a) Explain the various program memory addressing in 8086.

(b) What is meant by Stack? Explain its functions.

15. Explain with neat block diagram the system connections and signals associated with 80286 processor.

Or

16. Explain the features of protected mode of operation in 80286 and the switching over to protected mode from real mode.

17. (a) What are descriptors and selectors?

(b) Explain the memory management in 80386.

Or

18. (a) How interrupts and exceptions are handled in 80386?

(b) What is meant by task switching?

19. With block diagram, explain clearly the superscalar architecture of pentium processors.

Or

20. Write short notes on :

(a) MMX technology.

(b) Five stage instruction pipeline.

(c) Branch Prediction Logic.

(5 × 12 = 60 marks)

G 5209 (Pages : 2) Reg. No.....................................

Name...................................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : Electronics and Communication Engineering

TELEVISION ENGINEERING (L)

(Regular/Supplementary)

Time : Three Hours Maximum : 100 Marks

Answer all questions.

Part A

Each question carries 4 marks.

1. What is flickering effect ? Explain a method to overcome it.

2. Explain about horizontal and vertical resolution in 625 line system.

3. What is purity ? How it can be achieved in colour TV ?

4. Write the characteristics of delta gun picture tube.

5. Explain the need of AGC in TV receiver.

6. Explain the processing of sync. signal receiver.

7. What is colour burst signal ? What is the need of colour burst ?

8. What are the features of PAL system ?

9. Write a short note on HDTV.

10. Explain about LNB.

(10 × 4 = 40 marks)

Part B

Each question carries 12 marks.

11. Draw the basic block diagram of a TV transmitter and receiver and explain the different blocks.

Or

12. What is VSB transmission ? What are the advantages ? Also explain how a channel bandwidth of TMHz is achieved in 625 line system.

13. With a neat diagram explain the working of image orthicon tube.

Or

14. What is positive and negative modulation ? Also explain the advantages of negative modulation.

15. (a) Explain about a yagi-uda Antenna.

    (b) With a neat circuit diagram explain the working of delayed AGC system.

Or

16. Explain about the VSB correction applied to the signal in TV receiver. Also explain the need for this correction.

17. With a neat block diagram explain the working of NTSC coder.

Or

18. With a neat block diagram explain the working of PAL decoder.

19. Explain about :

    (a) VCD.

    (b) DVD.

    (c) Cable converter.

Or

20. With a block diagram explain about CCTV.

(5 × 12 = 60 marks)

G 5235

Reg. No............................

Name................................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : ECE/Applied Electronics and Instrumentation Engineering

VHDL (Elective II) (LA)

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

Answer all questions.

Part A

Each question carries 4 marks.

1. Write a note on IEEE 1164 value system for signals.

2. Write a note on identifiers in VHDL ?

3. Write a note on WAIT statements.

4. Realise the behavioral model of a 4 : 1 mux using VHDL.

5. With suitable examples, explain component instantiation ?

6. Compare the use of configuration specifications and configuration declarations ? Where is one or other advantageous.

7. Describe explicit visibility.

8. Write a note on sequential and concurrent procedure calls ?

9. Using generate statement, describe the model of a 16 bit shift regular using positive edge triggered FF ?

10. Describe the different test bench types.

(10 × 4 = 40 marks)

Part B

Each question carries 12 marks.

11. Explain the design units used in VHDL for hardware *abs* traction of a digital system.

Or

12. Explain the object types of predefined operators used in VHDL.

13. Explain with suitable examples, different delay models used in VHDL. How does these influence the synthesis of the design ?

Or

Turn over

14. Describe a 16 : 4 priority encoder with highest priority for 0, then prime numbered in the increasing order then others, using data flow model and behaviour model.

15. With suitable examples, discuss function signal attributes and signal kind attributes ?

Or

16. Describe the structural model of a 4 bit full adder.

17. With suitable examples, explain procedure calls ?

Or

18. With suitable example, explain how a package is declared and used in VHDL.

19. Write a full test bench for a 4 bit adder.

Or

20. Write a VHDL code to model a circuit that detects even no : of ones followed by odd number of zeros. Overlapping sequences are to be considered.

(5 × 12 = 60 marks)

G 5236

(Pages : 2)

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : Electronics and Communication Engineering/Applied Electronics and Instrumentation Engineering

ADVANCED MICROCONTROLLERS (Elective II) [LA]

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions.*

Part A

Each question carries 4 marks.

1. What are the characteristics of ATTiny 15 L controller ?
2. How do you vary the speed of operation of a controller ?
3. Identify the function of a watch dog timer.
4. Define resolution of an ADC.
5. Illustrate the concept of in system programming.
6. Enumerate the functions of event capture mode.
7. Identify the importance of a pre scalar.
8. What is the need for a micro-wire interface ?
9. Why does a flash memory get its name ?
10. Define SPI mode.

(10 × 4 = 40 marks)

Part B

Each question carries 12 marks.

11. Write a note on the features of Atmel AVR family controllers.

Or

12. With examples, write a note on the different addressing modes of ATTiny 15 L controller.

13. Write a note on EEPROM. Briefly describe the different methods used for reading and writing data into the EEPROM.

Or

14. Briefly describe the different functins of port B in Atmel controller.

Turn over

15. With a block diagram, explain the features of COP8CBR9 processor.

Or

16. Write a note on the different operating modes of the timers of COP 8 family.

17. Briefly describe dual clock operation and multi input wake up mode.

Or

18. What is an interrupt ? Describe the methods by which it is handled by the controller.

19. Describe the memory organization of a PIC processor.

Or

20. Write a note on I/O ports and the mode of operation of different ports of a PIC processor.

(5 × 12 = 60 marks)

G 5268

(Pages : 2)

Reg. No..............................

Name.................................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : Electronics and Communication/Applied Electronics and
Instrumentation Engineering

ADVANCED DIGITAL SIGNAL PROCESSING (Elective III) (LA)

(Regular/Supplementary)

Time : Three Hours

Maximum : 100 Marks

Answer **all** *questions.*

Part A

Each question carries 4 marks.

1. What is the need of decimating filter in a multirate signal processing system ?

2. Explain one practical application where a decimator is employed.

3. Compare adaptive and non-adaptive filters.

4. Write the weight update equation for a Weiner filter. Explain the parameters used.

5. Explain how the Hilbert transformation can be determined from the complex Fourier transform.

6. Explain briefly one application of DCT.

7. Explain the properties associated with a mother wavelet.

8. Sketch and mathematically express a Mexicon hat wavelet.

9. Explain the advantages of having Cache memory. What is meant by one-chip cache ?

10. Compare Harrard and non-Harrard architectures.

(10 × 4 = 40 marks)

Part B

Each question carries 12 marks.

11. Design a three stage decimator system to reduce the sampling rate from 1536 kHz to 16 kHz. Compute the MPS and TSR for the design. Indicate the assumptions used, such as filter specifications.

Or

12. (a) With a block diagram, explain sampling rate interpolation by a factor of 3/2.

    (b) Explain the applications of multirate signal processing.

13. (a) Derive an equation for the error performance for a Weiner filter. What is its minimum value and when it occurs ?

    (b) With a schematic explain adaptive echo canceller.

Or

Turn over

14. (a) Explain RLS algorithm.

    (b) Compare LMS and RLS algorithms.

15. (a) Define 2D Fourier and Inverse Fourier transforms.

    (b) Explain the applications of Gabor transform.

Or

16. (a) Discuss the properties of Fourier transforms.

    (b) Explain the limitations of short time Fourier transforms.

17. (a) Explain dyadic wavelet transform.

    (b) Explain inverse CWT.

Or

18. Explain multiresolution analysis.

19. (a) Explain special instructions used in typical DSP chip.

    (b) What is meant by superscalar architecture ? Illustrate with example.

Or

20. (a) Explain the concept of pipelining.

    (b) With a diagram, explain the MAC unit inside a typical DSP processor.

(5 × 12 = 60 marks)

G 5270 (Pages : 2) Reg. No...............................

Name.................................

B.TECH. DEGREE EXAMINATION, MAY 2013

Eighth Semester

Branch : Electronics and Communication Engineering/AE and I(Electronics and Instrumentation Engineering

MULTIMEDIA SYSTEMS (Elective III) [LAS]

(Regular/Supplementary)

Time : Three Hours   Maximum : 100 Marks

Answer **all** *questions.*

Part 'A'

Each question carries 4 *marks.*

1. Differentiate between Analog and Digital video.

2. Discuss some applicatins of multimedia.

3. What is hypertext ? Explain.

4. Explain what are fractals.

5. Write notes on quicktime.

6. Explain what is a multimedia PC.

7. Explain what is meant by composition in multimedia programming.

8. What is the purpose of using media classes ? Explain.

9. What is virtual reality ? Mention its uses.

10. Write notes on desktop video conferencing.

(10 × 4 = 40 marks)

Part B

Each question carries 12 *marks.*

11. (a) Explain the various features of multimedia authoring tools.

    (b) Explain any *two* multimedia output devices.

Or

12. Explailn the various storage devices for multimedia.

13. (a) Discuss the limitations of human perception that makes image compression possible.

    (b) Compare image compression with text compression.

Or

14. Write notes on (i) MPEG ; (ii) Fractals ; (iii) Animation.

Turn over

15. Discuss the members of CD family.

Or

16. Write notes on (i) DVI ; (ii) MME.

17. Explain the use of the various classes for multimedia programming.

Or

18. Discuss the various problems related to multimedia programming.

19. What is image synthesis ? Explain its potential in multimedia applications.

Or

20. Explain your concepts on what the future holds for multimedia. Justify your point of view.

(5 × 12 = 60 marks)