Reg No.:_____ Name:_____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

B.Tech S4 (S) Exam Sept 2020

Course Code: EE204

Course Name: DIGITAL ELECTRONICS AND LOGIC DESIGN (EE)

Max. Marks: 100 Duration: 3 Hours

PART A

Answer all questions, each carries 5 marks Marks

1		Convert	
	a)	$(2469)_{10}$ in to BCD.	(1)
	b)	$(735)_8$ to decimal.	(1)
	c)	$(650)_{10}$ to hexadecimal, gray and binary.	(3)
2		Using Boolean algebra prove that (A + B) (A'+C) = AC +A'B.	(5)
3		Design a full subtractor logic circuit.	(5)
4		Explain SISO and SIPO shift registers.	(5)
5		Draw the logic diagram and timing sequence of a 4-bit ring counter.	(5)
6		Prepare the state table and derive the logic expression for each flip flop input for a 3-bit binary synchronous down counter using T flip flop?	(5)
7		Explain the working of R-2R ladder type DAC.	(5)
8		Compare PAL and PLA.	(5)

PART B

Answer any two questions, each carries 10 marks

9	a)	Given X= 38_{10} and Y= 105_{10}. Using 2's complement method calculate (i) X-Y (ii) Y-X	(5)
	b)	How is the error detection and correction carried out using parity method in digital data transmission?	(5)
10	a)	Using K map, minimize the expression $F(A,B,C,D) = \sum m(1,2,3,8,14,15) + d(0,4,6,10)$.	(5)
	b)	Realize the Boolean expression Z=ABC + AD + CD' using NAND gates only.	(5)
11	a)	Explain a CMOS NAND gate .	(5)
	b)	Find the standard Product of Sum (POS) for the logic expression F=(A + B'C) C	(5)

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PART C

Answer any two questions, each carries 10 marks

12 Develop a 3-stage carry look ahead adder and implement using basic gates. (10)

13 Realize the following function F(A,B,C,D) = ∑m(1,3,4,10,11,12,13) using

(i) 4 X 1 MUX (ii) 8 X 1 MUX (10)

14 a) Explain a 3 bit asynchronous up counter. Draw the timing diagram and truth table. (5)

b) Draw the logic diagram of J-K flip flop and explain it. What is the advantage of J-K flip flop over S-R flip flop. (5)

PART D

Answer any two questions, each carries 10 marks

15 Design a 3-bit gray code synchronous counter using J-K flip flop and explain the steps in detail. (10)

16 a) Compare Mealy and Moore state machine models with example. (5)

b) Differentiate between ROM and RAM. (5)

17 a) Implement a full adder circuit using VHDL (5)

b) Explain the working of successive approximation ADC. Mention the advantages and disadvantages. (5)

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