

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
Fourth Semester B.Tech Degree Examination July 2021 (2019 Scheme)

Course Code: EET206

Course Name: DIGITAL ELECTRONICS

Max. Marks: 100

Duration: 3 Hours

PART A

(Answer all questions; each question carries 3 marks)

		Marks
1	Convert a) $(7483)_{10}$ into hexadecimal b) 1 1001 0100 into Gray Code	(3)
2	Realize NOT, AND and OR gate using NAND gates only.	(3)
3	State and explain DeMorgan's theorem.	(3)
4	Prove that $A+A'B=A+B$.	(3)
5	Draw a 4-bit gray to binary code converter circuit.	(3)
6	Draw the block diagram of ALU.	(3)
7	Explain Preset and Clear inputs of a flip-flop.	(3)
8	Draw the logic diagram of a 4 bit Johnson counter and explain its working.	(3)
9	Draw and explain R-2R ladder type DAC	(3)
10	Differentiate between PLA and PAL	(3)

PART B

(Answer one full question from each module, each question carries 14 marks)

Module -1

- 11 a) Subtract 46 from 99 using 1's complement and 2's complement methods. (7)
Compare both methods.
- b) Draw and Explain TTL NAND gate implementation (7)
- 12 a) With neat diagram, explain the operation of CMOS NOR gate. (7)
- b) Explain the error detection using parity method in digital transmission. Discuss (7)
how odd parity error detection carried out for transmitting the letter 'B' in ASCII code.

Module -2

- 13 a) Design a full subtractor circuit using basic gates. (7)
b) Reduce the expression using K map, (7)
 $F(A,B,C,D) = \sum m(6,7,8,10,11,15) + d(0,2,3,4,5,9,14).$
- 14 a) Draw and explain four bit parallel adder/subtractor circuit. (6)
b) Express $F(A,B,C,D) = \overline{A + B\bar{C} + C} + A\bar{C}$ in standard SOP and POS forms. (8)

Module -3

- 15 a) Realize a 2-bit comparator circuit. (8)
b) Implement the function $F(A,B,C,D) = \sum m(0,2,4,7,9,14)$ using 4 X 1 MUX. (6)
- 16 a) Differentiate decoder and encoder. Design a BCD to decimal decoder circuit. (8)
b) Design an even parity generator circuit for 3-bit messages. (6)

Module -4

- 17 a) Design a mod-12 asynchronous counter using J-K flip flops. Draw the timing diagram. (8)
b) Explain different types of shift registers. (6)
- 18 a) Design mod-14 synchronous counter using T-flip flop by explaining the steps in detail. (10)
b) Convert J-K flip-flop to T flip-flop. (4)

Module -5

- 19 a) Compare Mealy and Moore state machine models with example. (6)
b) Explain the working of (8)
(i) successive approximation ADC and
(ii) Flash type ADC.
- 20 a) Implement the function $F(A,B,C,D) = \sum m(3,7,8,9,11,15)$ using PLA (6)
b) Implement AND gate and a half adder circuit using VHDL. (8)
