

Reg No.: _____

Name: _____

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Sixth Semester B.Tech Degree Regular and Supplementary Examination July 2021

Course Code: EC304**Course Name: VLSI**

Max. Marks: 100

Duration: 3 Hours

PART A*Answer any two full questions, each carries 15 marks*

Marks

- 1 a) With a neat sketch, explain Czochralski crystal growth mechanism. (8)
 b) Explain the N-well CMOS IC Fabrication Sequence. (7)
- 2 a) After a pre-deposition step, it is found that 5×10^{15} phosphorus atoms cm^{-2} are introduced in a p-type silicon sample doped with 10^{16} acceptor atoms cm^{-3} . Calculate the junction depth, when the drive-in diffusion is performed at 1200°C for two hours. ($D=2.5 \times 10^{-12} \text{ cm}^2/\text{s}$ at 1200°C). (7)
 b) With a neat sketch, explain the process of vapour phase epitaxy. (8)
- 3 a) Solve the Fick's law of diffusion, corresponding to pre-deposition diffusion and drive in diffusion. (8)
 b) Explain the process of molecular beam epitaxy (MBE) in detail. (7)

PART B*Answer any two full questions, each carries 15 marks*

- 4 a) Explain the various types of power dissipation in CMOS inverter. (9)
 b) Realize an XNOR gate using (6)
 i. NMOS pass transistor logic
 ii. Complementary pass transistor logic
- 5 a) Draw the circuit diagram, stick diagram and layout of a CMOS NOR gate (8)
 b) Implement the function $Y = A'B + AB'$ and $Z = AB + A'B'$ using pass transistor logic. (7)
- 6 a) Explain the working of a transmission gate and implement 4×1 multiplexer using transmission gates. (9)
 b) Implement the function $Y = [(A+B)C + DE]$ using static CMOS logic (6)

PART C*Answer any two full questions, each carries 20 marks*

- 7 a) Explain the read and write operation of a six transistor CMOS SRAM cell. (10)

- b) With block diagrams, explain the working of linear carry select adder and square root carry select adder. (10)
- 8 a) Design a 4-bit \times 4-bit NAND-based ROM array and explain its working. (10)
- b) With necessary diagrams and equations, explain the design of carry bypass adders (10)
- 9 a) Draw a neat block diagram and discuss the operation of 4 \times 4 bit-array multiplier. (10)
- b) Design a 4-bit \times 4-bit NOR-based ROM array and explain its working. (10)
