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B.TECH. DEGREE EXAMINATION, APRIL 2010

Sixth Semester

Branch: Electrical and Electronics Engineering

CONTROL SYSTEM—I (E)

(Regular-2007 admissions; Supplementary-Prior to 2007 admissions)

Time: Three Hours

Maximum: 100 Marks

Part A

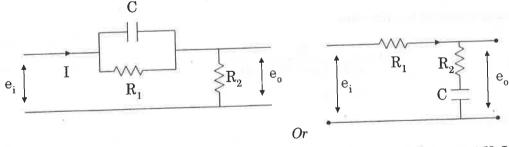
Answer all the questions. Each question carries 4 marks.

- 1. Explain the application of Laplace transform to control systems.
- 2. Explain the Mason's gain formula.
- 3. Define and explain type and order of a system.
- 4. Define Error constants.
- 5. What is asymptotic stability? Explain in detail.
- 6. Explain the advantages and applications of root locus technique.
- 7. What is Bode plot? Explain in detail.
- 8. Differentiate phase margin from gain margin.
- 9. What are synchros? Explain.
- 10. Explain the chracteristics of tachogenerators.

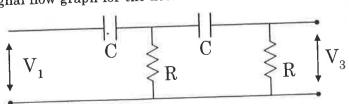
 $(10 \times 4 = 40 \text{ marks})$

Part B

11. Find the transfer functions of the following networks:



12. Draw the signal flow graph for the network shown below and hence find V_3/V_1 .



Turn over

13. Define and explain the time domain specifications.

Or

14. The open-loop transfer function of an unity feedback control system is given by

$$C(s) = \frac{100}{s(s+2)(s+5)}$$
.

For unit step input, find the time response of the closed loop system and determine percentage overshoot and the rise time.

15. Construct the root locus for the given function and find τ for K=2.

$$GH(s) = \frac{K}{(s+1)(s^2+4s+4)}.$$

Or

16. Explain Routh's Hurwitz stability criterion. Choose the real value of K so that the system is just oscillatory for the function:

$$F(s) = s^4 + Ks^3 + (K+4)s^2 + (K+3)s + 4 = 0.$$

17. Draw the Bode plots for the function

$$G(s) = \frac{(1 + sTa) (1 + sTb)}{(1 + sT_1) (1 + sT_2)}$$

where $T_1 > T_a > T_b > T_2$.

Or

- 18. Find the gain margin and phase margin for $HG(s) = \frac{2(s+1)}{s^2}$. Also find w.
- 19. Find the breakaway point for the function

$$GH(s) = \frac{K}{s(s+1)(s+3)(s+4)}.$$

Or

- 20. Write technical notes on:
 - (a) Gyroscopes.

(4 marks)

(b) Rotating amplifiers.

(4 marks)

(c) Amplidyne.

(4 marks)

 $[5 \times 12 = 60 \text{ marks}]$

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B.TECH. DEGREE EXAMINATION, APRIL 2010

Sixth Semester

Branch: Electrical and Electronics Engineering

ELECTRICAL MACHINES—II (E)

(Regular-2007 admissions; Supplementary-Prior to 2007 admissions)

Time: Three Hours

Maximum: 100 Marks

Answer all questions.

Part A

- 1. Explain single layer and double layer winding.
- 2. Explain revolving magnetic field.
- 3. Explain "effects of harmonics on pitch and distribution factors'.
- 4. Draw the circuit model of synchronous machine.
- 5. Explain how proper synchronization is achieved in alternators.
- 6. Explain the principle of operation of synchronous motor.
- 7. Explain the construction of 'V' curves.
- 8. What is synchronous condenser?
- 9. Compare synchronous and induction motors.
- 10. Explain the principle of operation of Brushless Alternators.

 $(10 \times 4 = 40 \text{ marks})$

Part B

11. (a) The stator of 3-phase, 16 pole alternator has 144 slots and there are 4 conductors per slot connected in two layers and the conductors of each phase are connected in series. If the speed of the alternator is 375 r.p.m, calculate the e.m.f. generator per phase. Resultant flux in the air gap is 5×10^{-2} webers/pole sinusoidally distributed. Assume coil span 150°.

(6 marks)

(b) Explain constructional features of salient pole machines.

(6 marks)

Or

12. (a) Draw and explain different types of armature winding.

(6 marks)

(b) What is meant by phase grouping?

(6 marks)

13. (a) Explain parallel operation of alternators.

(6 marks)

(b) Discuss about synchroscope.

(6 marks)

Or

 $(5 \times 12 = 60 \text{ marks})$

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B.TECH. DEGREE EXAMINATION, APRIL 2010

Sixth Semester

Branch: Electrical and Electronics Engineering

ELECTRICAL POWER TRANSMISSION (E)

(Regular-2007 admissions ; Supplementary-Prior to 2007 admissions)

Time: Three Hours

Maximum: 100 Marks

Answer all questions.

Part A

- 1. Define "skin effect" and peroximity effect in transmission line.
- Explain the effect of earth on line capacitance.
- Short note on "testing of insulators".
- What is Damper? Explain.
- Describe tap changing transformer.
- Explain the need of voltage control in transmission line.
- What is corona? Explain the various methods used to reduce corona.
- Explain the reactance earthing in detail.
- What are the limitations of EHV AC transmission?
- 10. What are the advantages of HVAC transmission?

 $(10 \times 4 = 40 \text{ marks})$

Part B

11. Derive the inductance of three-phase line with unsymmetrical spacing.

- Derive the capacitance of three-phase line with symmetrical spacing.
- What is Line insulator? Explain its types in detail.

Or

14. (a) What is sag? Explain.

(4 marks)

- (b) A three-phase line is supported by a string of three similar insulators. If the voltage across the lowest unit is $20\,\mathrm{kV}$, shunt capacitance between earth and insulator is $1/20^\mathrm{th}$ of the capacitance insulator. Find the line voltage. (8 marks)
- 15. Derive the ABCD constants and phase diagram of a transmission line.

	G 2194
16. (a) Explain Ferranti effect.	(4 marks)
(b) Explain the analysis of medium line by T method.	(8 marks)
17. (a) Discuss the radio interference effect of power transmission line.	(6 marks)
(b) Explain the method used for measuring earth resistance.	·
	(6 marks)
18. Short notes on:	
(a) Lower footing resistance.	(4 marks)
(b) Neutral grounding.	(4 marks)
(c) Grounding transformer.	(4 marks)
19. What is EHV transmission? Explain in detail.	()
Or	
(a) Graztz circuit.	
(b) EHV systems in India.	
	(6 marks)
	$5 \times 12 = 60$ marksl

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B.TECH. DEGREE EXAMINATION, APRIL 2010

Sixth Semester

Branch: Electrical and Electronics Engineering
DIGITAL SIGNAL PROCESSING (E)

(Regular-2007 admissions; Supplementary-Prior to 2007 admissions)

Time: Three Hours

Maximum: 100 Marks

Answer all questions.

Part A

Each question carries 4 marks.

1. List out the advantages and disadvantages of DSP.

2. List out any four properties of DFT.

3. Distinguish between linear and circular convolution of two sequences.

4. What is FFT? Why FFT is needed?

5. State the initial value theorem and the final value theorem.

6. Draw the parallel form structure of IIR filter.

7. What are the desirable and undesirable features of FIR filters?

8. What is the principle of designing FIR filter using frequency sampling method?

9. What is meant by impulse invariant method of designing IIR filter?

10. Give the equation for the order of N and cut-off frequency ΩC of Butterworth filter.

 $(10 \times 4 = 40 \text{ marks})$

Part B and the gradual amother from moving and the

Each question carries 12 marks.

11. (a) Explain the classifications of Discrete time systems.

(4 marks)

(b) Determine the convolution of two sequences:

$$x(n) = \{3, 2, 1, 2\}, h(n) = \{1, 2, 1, 2\}$$

(8 marks)

Or

12. (a) State and prove the convolution property of DTFT.

(6 marks)

(b) Find the Fourier transform of $x(n) = \left(\frac{1}{2}\right)^{n-1} u(n-1)$.

(6 marks)

Turn over

13. Compute 4-point DFT of the following sequences using (a) DIT; (b) DIF algorithm:

$$x(n) = \{1, 2, 3, 4\}$$

$$x(n) = \{1, 1, -1, -1\}.$$

(12 marks)

Streit Semester

Bratich : Electrical and Plactronics Engineering 14. Explain the properties of DFT.

(12 marks)

15. (a) Find the inverse z-transform of $X(z) = \log(1 - 0.5z^{-1}); |z| > 0.5$ using differentiation property. Maximum; 100; Mucha

(6 marks)

(b) Find the z-transform of
$$x(n) = \left(-\frac{1}{5}\right)^n u(n) + 5\left(\frac{1}{2}\right)^{-n} u(-n-1)$$
.

(6 marks)

Obtain the direct form I, II, cascade form, parallel form for

$$y(n) = \frac{5}{6} y(n-1) + \frac{1}{6} y(n-2) = x(n) + 2x(n-1).$$
 (12 marks)

Determine the filter co-efficients h(n) obtained by sampling:

$$Hd(e^{jw}) = e^{-j(N-1)w/2}, \quad 0 \le |w| \le \pi/2$$

The first of the property of the π and π and π and π are the second of the π What is meant by impulse invariant intribod of designing IIR filler ?

for N = 7.

 Give the equation for the order of N and dut of frequency OC of Butterworth filter. 18. Explain FIR filter design using windows.

(12 marks)

19. For the given specifications design an analog Butterworth filter:

$$0.9 \le |H(j\Omega)| \le 1 \text{ for } 0 \le \Omega \le 0.2 \pi$$

 $|H(j\Omega)| \le 0.2 \text{ for } 0.4\pi \le \Omega \le \pi.$

secures pre over to quitulovaco ade scrimtered (12 marks)

 $(\mathbb{R}, \mathbb{L}, \mathbb{R}, \mathbb{L}) = (nOr, (\mathbb{R}, \mathbb{L}, \mathfrak{L}, \mathbb{R})) = (nOr, (\mathbb{R}, \mathbb{L}, \mathfrak{L}, \mathbb{R}))$

20. Describe the features of TMS320C family processor with neat diagram.

(12 marks)

 $[5 \times 12 = 60 \text{ marks}]$

(coltain b)

(b) Find the Fourier transform of $x(n) = \left(\frac{1}{2}\right)^{n-1} u(n-1)$.

12. (a) State and prove the eduvelation property of DTFT.

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Explain stack soints and stack operation with example

B.TECH. DEGREE EXAMINATION, APRIL 2010

Sixth Semester

Branch: Electrical and Electronics Engineering

MICROPROCESSOR AND APPLICATIONS (E)

(Regular-2007 admissions; Supplementary-Prior to 2007 admissions)

Time: Three Hours

Maximum: 100 Marks

Answer all questions.

20. Draw the internal architecture of 8086 A rarq

Each question carries 4 marks.

- 1. Explain T state, machine cycle and instruction cycle.
- 2. Draw and explain 8085 bus structures.
- 3. Discuss classifications of 8085 instructions.
- 4. Write a 8085 program to generate a delay of 0.6 Sec for the given crystal frequency of 5 MHz.
- 5. Define stack pointer and stack.
- 6. Explain 8085 interrupts.
- 7. Differentiate memory mapped I/O and I/O mapped I/O.
- 8. Explain the features of 8255.
- 9. Write short notes on interfacing microprocessor to stepper motor.
- 10. Compare 8085 microprocessor with 8086 processor.

 $(10 \times 4 = 40 \text{ marks})$

Part B

Each question carries 12 marks.

11. Draw the architecture of 8085 microprocessor and explain main parts in it.

Or

- 12. Draw the timing diagram for MVI A, 08.
- 13. (a) Write a program to arrange numbers in descending order.

(6 marks)

(b) Write a assembly level program and multiply 2, 8-bit numbers.

(6 marks)

0

14. (a) Write a program to find a greatest number in an array.

(6 marks)

(b) Write a program to divide two 8 bit numbers.

(6 marks)

15. Explain stack pointer and stack operation with example.

16. (a) What are the types of interrupts in 8085? Explain in detail the hardware interrupts. Sixth Semester .

(6 marks)

(b) What do you mean by polling in 8085? The feoretes in doment

(6 marks)

17. Explain the I/O mode operation of 8255 in detail.

Explain the interfacing of Alpha numeric displays to Microprocessors.

Explain how ADC chip can be interfaced with Microprocessor.

Answer of questions

20. Draw the internal architecture of 8086.

 $[5 \times 12 = 60 \text{ marks}]$

(b) Write a assembly level program and multiply 2, 8-bit numbers.

G 222	(Pages: 2)	Reg. No
		Name Explain the following
(4 marks)	D. IECH. DEGREE EXAMINATION	APRIL 2010 (d)
(4 marks) (4 marks)	Sixth Semester	(c) E ² PROM.
	Branch: Electrical and Electronics	Engineering
	COMPUTER ORGANISATION	16. (a) Compare PAL with F(3) V
	and a second	rior to 2007 admissions)
Time · Th	nisation of memory chips.	Maximum: 100 Marks
11110.11	Answer all questions.	
	Part A	18. Explain the following:
	Each question carries 4 mark	(a) Cache memoryss (b) Associative mapping.
	hat is microprogrammed control? Explain. iscuss bus structures.	19. Explain how CPU handles mult
article and the second second second	I lain the circuit diagram of 2's complement a	adder.
	That is meant by one stage ALU? Explain.	20. Explain RS232 and RS423 bus
[ax 5. D	iscuss Flash memory.	
6. W	That are the applications of FPLA?	
7. W	That is meant by memory interleaving?	
	iscuss mapping functions.	
9. W	That is synchronous asynchronous buses?	
10. E	xplain DCI.	$(10 \times 4 = 40 \text{ marks})$
	Part B	
	Each question carries 12 ma	rks.
11. D	raw the functional block diagram of digital computer an	nd explain each block in its.
	Or	
12. (a	a) Compare Microprogrammed control and hardwired c	
(b	o) Discuss about typical operation cycle.	(6 marks)
13. E	Explain the operation of serial and parallel adder circuit	with neat diagram.
14 15	Explain multiplication and division operations.	
14. E	explain multiplication and division operations.	

******		(Pag ² s: 2) Reg. No	20	G 222
15.	Explain	in the following :—		
	(a)	STECH. DEGREE EXAMINATION, APRIL 2010.	(4	marks
	(b)	Auxiliary memory.		marks
	(c)	E ² PROM. Semester	(4	marks
		Branch : Electrical and Of lectronics Engineering		
16.	(a) Co	COMPUTER ORGANISATION ALI diw LAS arapmo	(6	marks
	(b) Ex	xplain simple programmable logic devices any one. Toos-	6) (Regular-	marks
2×17;		and explain internal organisation of memory chips.	hree Hours	
		Answer an Questions.		
18.	Explain	n the following -		
	(a)	Cache memory.	16	marks
	(b)	Associative mapping.		marks
19.	Explain	n how CPU handles multiple devices.		-4
		netures.	Discuss bus str	
20.	Explain	n RS232 and RS423 bus standards.		
		by one stage ALU : Explain.		
			$[5 \times 12 = 60]$	
		upplications of FPLA?		
		by memory interleaving 2		
			Discuss mappi	
		ronous asynchronous buses?		
	01 - 1	war.	Explain DCL	10.
narks)	4 = 40 n			
*		- Part B		
		Each question carries 12 marks.		
		tional block diagram of digital computer and explain each block in it	Draw the fund	11.
		10		
narks)	(6 n	Microprogrammed control and hardwired control.	(a) Compare	12. (
narks)	(6 n	oout typical operation cycle.	(b) Discuss a	
		eration of serial and parallel adder circuit with neat diagram.	Explain the op	13.
		10		
		dication and division operations.	Explain multip	14.

Turn over