F 6259 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2013

Third Semester

Branch : Common for all Branches

EN 010 302—ECONOMICS AND COMMUNICATION SKILLS

(AI, AN, AU, CE, CS, EC, EE, EI, IC, IT, ME, MT, PE and PO)

(New Scheme—Regular/Improvement/Supplementary/)

Time : Three Hours Maximum : 100 Marks

Answer **all** *questions.*

Part A

Each question carries 3 *marks.*

1. Mention any *six* Nationalised Banks.
2. What do you mean by an MNC ?
3. Explain the merits of direct tax.
4. Discuss the reasons for inflation.
5. What is TRIPS and TRIMS ?

(5 × 3 = 15 marks)

Part B

Each question carries 5 *marks.*

6. Discuss the importance of mutual funds.
7. Distinguish between Direct and Indirect taxes.
8. Explain the steps involved in tax evasion.
9. What is meant by demand pulls and cost push effects of inflation ?
10. Comment on the international trade systems.

(5 × 5 = 25 marks)

Part C

Each question carries 12 *marks.*

11. Explain the major roles of small scale industries (SSI).

Or

12. What are the problems facing by Indian stock markets (BSE and NSE) ?

Turn over

13. Discuss the effects of MNC's in the Indian economy.

Or

14. Explain the Government of Indian's policy on LPG. (Liberalisation Privatisation and Globelisation).

15. Explain the problems associated with deficit financing.

Or

16. What are the functions of tax system in India ? Discuss different types of indirect taxes.

17. Write notes on the following :

    (a) GNP.

    (b) NNP and

    (c) NI.

Or

18. Explain the methods of estimating National Income.

19. Explain the imparts of WTO decisions on Indian industry.

Or

20. Explain the different aspects of BOP (Balance of payments).

(5 × 12 = 60 marks)

F 6292 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2013

Third Semester

Branch : Information Technology

IT 010 305—PRINCIPLES OF COMMUNICATION ENGINEERING (IT)

(New Scheme—Regular/Improvement/Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 3 *marks.*

1. State the merits and demerits of superheterodyne receiver.
2. What is overmodulation ? How it can be overcome ?
3. An FM wave is defined by $f(t) = 10 \cos (10^6 \pi t + \sin 4\pi t)$. Calculate the instantaneous frequency of $f(t)$.
4. Explain shot noise.
5. Name two non-communication applications for PWM.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. With neat block diagram, explain microwave link.
7. An AM broadcast transmitter radiates 25 kW when the modulation index is 85 %. How much of this is carrier power ? Also compute the power of each side band.
8. Draw and briefly explain the block diagram of FM transmitter which uses a reactance modulator.
9. Calculate the thermal noise voltage generated by two resistors of 50 kΩ and 80 kΩ at 400 K, in series for a bandwidth of 150 kHz.
10. Explain, why PCM is more noise-resistant than the other forms of pulse modulation.

(5 × 5 = 25 marks)

Turn over

Part C

Answer any **one** *full question from each module.*
Each full question carries 12 *marks.*

Module I

11. With a neat block diagram, describe satellite communication system. What are its merits and demerits ?

Or

12. Draw a block diagram of a double superheterodyne receiver to receive a frequency range, say from 500 kHz to about 50 MHz. Explain the purpose and function of each block.

Module II

13. With the help of a block diagram and frequency spectrum, explain the generation of DSBSC waves.

Or

14. From fundamentals, derive the expression for AM wave. A sinusoidal carrier having amplitude of 10 V and frequency 300 kHz is amplitude modulated by sinusoidal signals of (i) 3V and 1000 Hz ; and (ii) 5V and 800 Hz. Sketch its frequency spectrum.

Module III

15. (a) Explain pre-emphasis and de-emphasis with appropriate circuit diagrams ? What are its need ?

(7 marks)

(b) Plot the frequency spectrum of a single tone wide band FM and explain. (5 marks)

Or

16. With the help of neat block diagram, explain the working of a FM broadcast transmitter. Why FM is more noise immune compared to AM ?

Module IV

17. (a) Define signal-to-noise ratio and noise figure of a receiver. When might the latter be a move suitable piece of information than the equivalent noise resistance ?

(b) An amplifier operating over the frequency range 455 to 460 kHz has a 200 kΩ input resistor. What is the r.m.s. noise voltage at the input to this amplifier if the ambient temperature is 17° C ?

Or

18. (a) Define the equivalent noise temperature of a receiver. Under what conditions could this be a more useful quantity than the noise figure ? Why ?

(7 marks)

(b) Explain, what double spotting is and how it arises. What is its nuisance value ? (5 marks)

Module V

19. Distinguish between PAM, PWM, PPM and PCM sketching their waveshapes. Bring out their important features and field of applications.

Or

20. With a neat block diagram, show how PCM can be generated. What is quantization noise ? How it can be minimised ?

(5 × 12 = 60 marks)

F 6301 **(Pages : 6)** **Reg. No.....**

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2013

Third Semester

Branch : Information Technology

ELECTRICAL CIRCUITS AND SYSTEMS (T)

(Old Scheme—Supplementary/Mercy Chance)

Time : Three Hours **Maximum : 100 Marks**

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks.*

1. Determine v_c, v_x and i_0 for $t > 0$, $v_c(0) = 30$ V for the circuit shown in Fig 1.

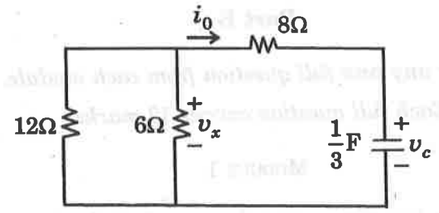

Fig. 1.

2. The voltage $v = 12 \cos(60t + 45°)$ is applied to a 0.1 H inductor. Find the steady state current through the inductor.
3. A series RL circuit with R = 10Ω, L = 0.01 H is energized by a source $v = 50 \sin(500t + 45°)$. Calculate the resulting current and find its value when $t = 0.01$ sec.
4. Define time constant of a series RC circuit A series RC circuit is energized by a d.c. source. Derive from basics and expression for the voltages across the capacitor at any time t.
5. Solve $\frac{d^4y}{dt^4} - k^4 y = 0$, given $y(0) = 1, y'(0) = y''(0) = 0$, use Laplace transforms.
6. Find the Laplace transform of
   (a) $\sin(wt)\,u(t)$. (b) $\cos(wt)\,u(t)$.
7. A Coil of R = 5Ω, L = 1H is connected in parallel with a capacitance $C = \frac{1}{2}$ F. Calculate the impedance function of the circuit.

Turn over

8. Find the Thevenin equivalent for the circuit shown in Fig. 2.

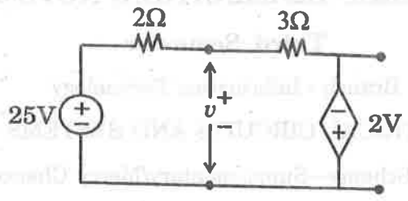

Fig. 2.

9. Explain the significance of poles and zeros of system transfer function on the time domain response.

10. Briefly explain open circuit impedance parameters and transmission parameters.

(10 × 4 = 40 marks)

Part B

Answer any **one** *full question from each module.*

Each full question carries 12 *marks.*

Module 1

11. (a) Using repeated source transformation theorem find the Norton equivalent circuit of the following Fig. 3.

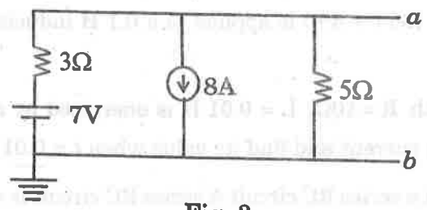

Fig. 3.

(b) The switch in the following circuit in Fig. 4 has been closed for a long time. At $t = 0$, the switch is opened. Calculate $i(t)$ for $t > 0$.

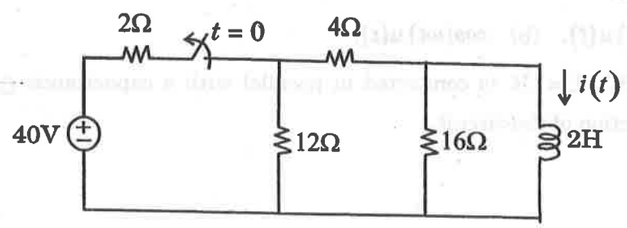

Fig. 4.

Or

MODULE 5

19. Find the transmission parameters of the network shown in Fig. 14.

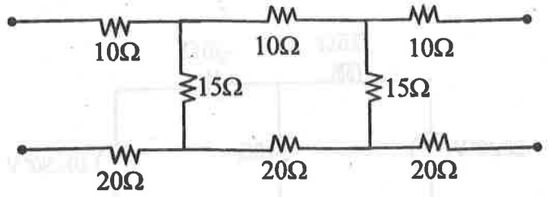

Fig. 14.

Or

20. The transform voltage of a network is $V(s) = \dfrac{3s}{(s+2)\left(s^2+2s+2\right)}$. Plot its pole-zero diagram and hence obtain $v(t)$.

(5 × 12 = 60 marks)

12. (a) In the circuit shown in Fig. 5. below, the switch S is closed at $t = 0$. Write the loop equations and solve for i_1 and i_2.

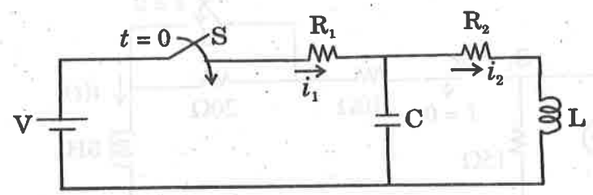

Fig. 5.

(b) In the coupled circuit of Fig. 6, find the net inductance.

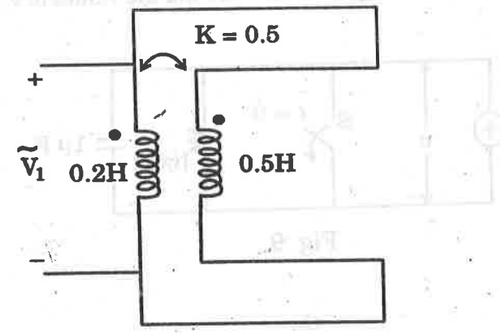

Fig. 6.

MODULE 2

13. The switch in the Fig. 7 has been in position A for a long time. At time $t = 0$, the switch moves to position B. Determine $v(t)$ for $t > 0$ and calculate its value at $t = 1$ sec and 4 sec.

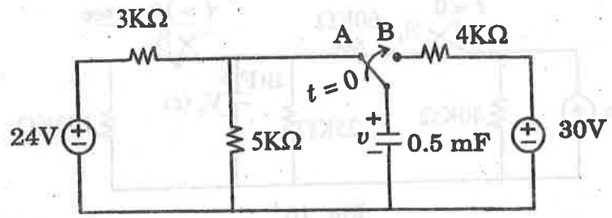

Fig. 7.

Or

14. The switch S_1 is closed at $t = 0$, and switch S_2 is closed at $t = 2$ sec. Calculate $i(t)$ for all t. Find $i(1)$ and $i(3)$.

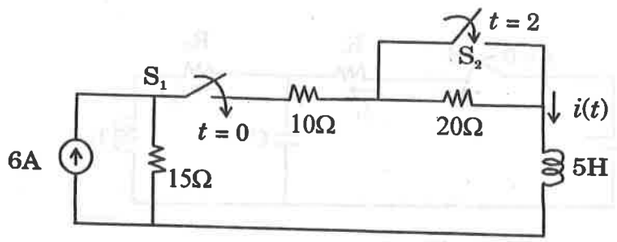

Fig. 8.

MODULE 3

15. In the circuit in Fig. 9, the switch S is opened at $t = 0$. Find the values of v, $\frac{di}{dt}$ and $\frac{d^2i}{dt^2}$ at $t = 0^+$.

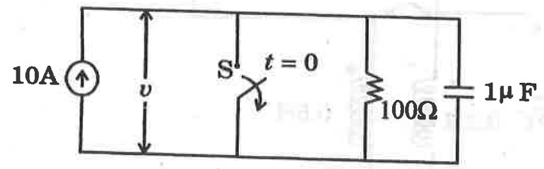

Fig. 9.

Or

16. In the circuit shown in Fig. 10, the switch S_1 has been open for a long time. At $t = 0$, the switch S_1 is opened. Then 10 msec later, the switch S_2 in closed. Find.

(a) $V_c(t)$ for $0 \le t \le 0.015$.

(b) $V_c(t)$ for $t \ge 0.015$.

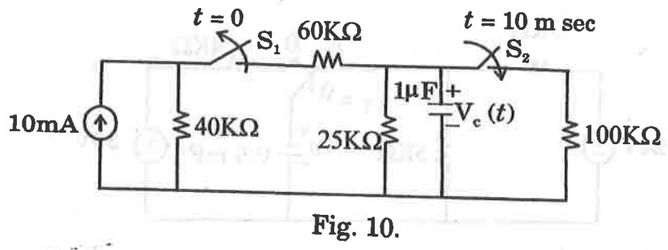

Fig. 10.

MODULE 4

17. (a) Determine the current through 10Ω resistance of the network shown in Fig. 11 using super position theorem.

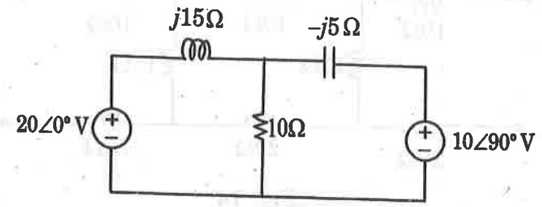

Fig. 11.

(b) Verify reciprocity theorem for the network shown in Fig. 12.

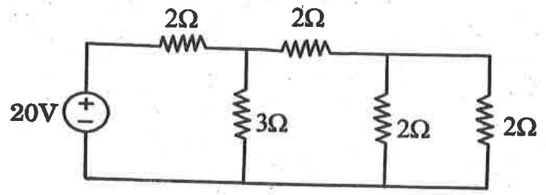

Fig. 12.

Or

18. Find Thevenin's and Norton's equivalents for the following circuit in Fig. 13.

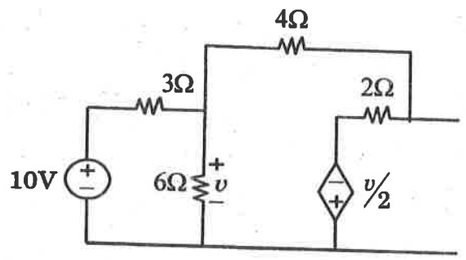

Fig. 13.

F 6334

(Pages : 3)

Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2013

Third Semester

Branch : Information Technology

DIGITAL ELECTRONICS (T)

(Old Scheme—Supplementary/Mercy Chance)

Time : Three Hours

Maximum : 100 Marks

Part A

Answer **all** *questions briefly.*
Each question carries 4 *marks*

1. Express the decimal 69 in :

   (a) Binary

   (b) Octal.

   (c) Hexadecimal.

   (d) Gray code.

   (e) BCD and

   (f) Excess-3 codes.

2. Convert the following in standard canonical forms :

   (a) $x + xy + xyz$ in SOP.

   (b) $(x + y)(x + z)$ in POS.

3. Draw and explain the block schematics of 8-bit parallel adder.

4. Explain how a multiplexer can be used as a logic function generator.

5. How is the switching speed of CMOS logic gate affected by increasing frequency ? Give reasons ?

6. Define and explain clearly current sinking and current sourcing, based on standard TTL gate ?

7. Show how an SR flip-flop can be converted to a D flip-flop ?

8. How is individual location in an EE PROM programmed or erased ?

9. A 4-bit modulo 16 binary up/down counter is in the state 0000. What is the next state in the (i) up mode ? and in the (ii) down mode ?

10. Why does a Johnson counter have decoding gates, where as a ring counter does not ?

(10 × 4 = 40 marks)

Turn over

Part B

Answer any **one** *full questions from each module.*
Each full question carries 12 *marks.*

MODULE 1

11. Reduce $S = \Sigma(1, 2, 4, 5, 6, 8, 9, 12) + d(3, 10, 13, 15)$ using Quine Mc cluskey method and draw the minimal circuit using fundamental logic gates.

Or

12. Using k-maps simplify the following Boolean expressions

(a) $f_1 = \bar{A}B\bar{D} + ACD + \bar{B}CD + BC\bar{D} + \bar{A}\bar{C}D$.

(b) $f_2 = \Sigma m(0, 2, 3, 4, 8, 10, 12, 13, 14)$.

MODULE 2

13. (a) Implement the following functions using decoder, minimizing the number of inputs to be summed

(a) $f_1 = \Sigma(0, 2, 3, 5, 6, 7)$.

(b) $f_2 = \Sigma(1, 3, 4, 6, 7)$.

(b) Implement the Boolean function $f = \Sigma m(0, 1, 5, 6, 7, 9, 12, 15)$ using 8 to 1 multiplexer.

Or

14. (a) Explain, with circuit diagram, the operation of a single digit BCD adder clearly.

(b) Realise a 5 : 32 decoder using 2 : 4 decoders and draw circuit diagram.

MODULE 3

15. (a) What is meant by open collector output of TTL gate ? What is its utility ? Draw its circuit and explain the advantages ?

(b) With a detailed circuit diagram, describe the working of a 3- input CMOS NAND gate.

Or

16. (a) What are the advantages of CMOS logic over NMOS logic ? Explain with example for each how to realise the boolean function using both types of logic ?

(b) Mention four different sublogic families in TTL ? Compare their typical power dissipation per gate and propagation delay.

MODULE 4

17. Give a general structure of PLA. Explain its advantages. Implement the following functions using 3 × 4 × 2 PLA

(a) $f_1 = \Sigma m(0, 2, 3, 4)$.

(b) $f_2 = \Sigma m(0, 1, 2, 4, 5)$.

Or

18. Explain how excitation tables are used in the design of clocked synchronous sequential network. Show how the excitation tables of JK and D flip-flops are obtained from their truth tables ?

MODULE 5

19. Draw the circuit diagram of a mod-14 count up ripple counter using count reset with timing diagram and function table explain the working.

Or

20. Explain the working of a serial in serial out shift register with logic diagram and wave forms.

(5 × 12 = 60 marks)