F 3571 (Pages : 6) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Third Semester

Branch : Information Technology

ELECTRICAL CIRCUITS AND SYSTEMS (T)

(Prior to 2010 Admissions—Old Scheme)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Draw the electrical equivalent of the coupled coils shown in Figure 1 and Figure 2.

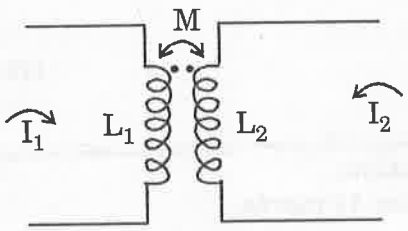


Fig. 1

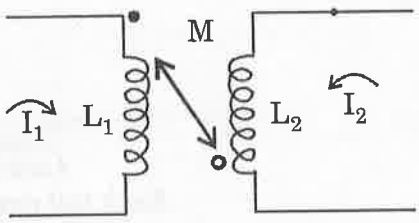


Fig. 2

2. State Dual network and dual graph.
3. Explain the term integrating factor.
4. Find the general solution for current i (t) for the RC. circuit shown in the Figure (3), the applied voltage E (t) being a constant electromotive force.

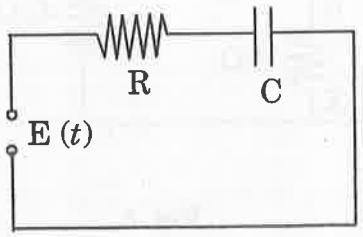


Fig. 3

Turn over

5. Explain the second order differential equation.
6. Explain how to get Laplace Transform of impulse function.
7. Compare complex frequency and natural frequency.
8. State Thevenins and Norton theorems.
9. Explain the significance of poles and zeros in network functions.
10. Compute the open - circuit impedance parameters for the T - network shown in Figure (4).

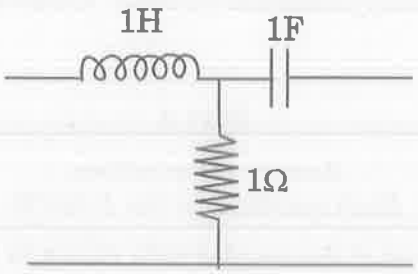


Fig. 4

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) Find the current through 10 V source in Figure 5 using injection of current sources and source transformation methods.

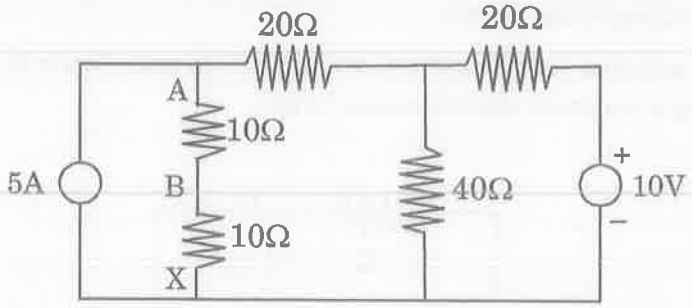


Fig. 5

(6 marks)

(b) For the following circuit shown in Figure (6), find $i(t)$ for $t > 0$ if the switch is opened at $t = 0$.

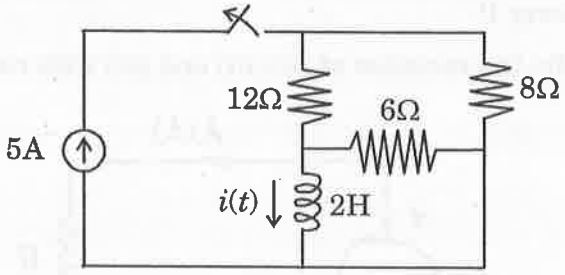


Fig. 6

(6 marks)

Or

12. (a) Find the loop currents in the network shown in the Fig. (7)

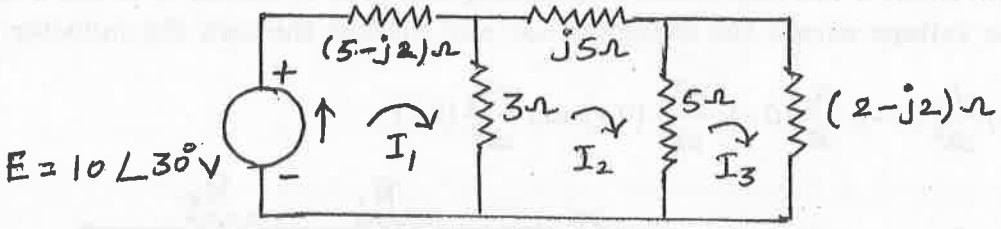


Fig. 7

(6 marks)

(b) Using the dual elements, obtain the dual network for the circuit shown in Figure (8)

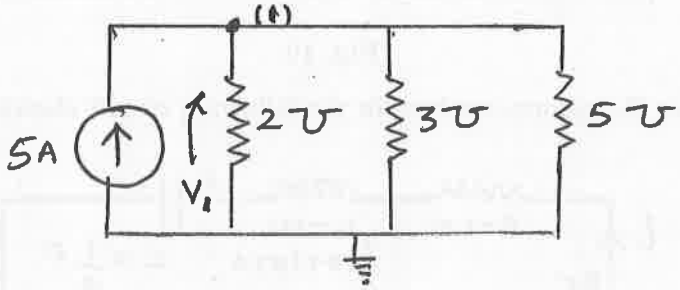


Fig. 8

(6 marks)

13. In the circuit shown in Fig. (9) the voltage function $v(t) = 100 \sin wt$ value and R = 25 ohms, find

(a) The current $i(t)$.

(b) Instantaneous power $p(t)$ and

(c) The average power P.

(d) Show graphically the variation of $v(t)$, $i(t)$ and $p(t)$ with respect to time.

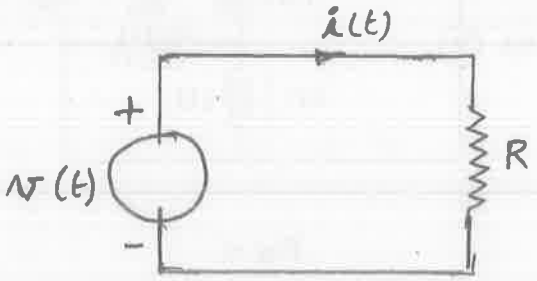


Fig. 9

(4 × 3 = 12 marks)

Or

14. Fig. (10) shows a two loop network. Assuming that prior to closing of switch k (at $t = 0$) there was no voltage across the capacitor nor any current through the inductor find $i_1(0+)$, $i_2(0+)$, $\frac{di_1}{dt^2}(0+)$, $\frac{di_2}{dt}(0+)$, $\frac{d^2i_1}{dt^2}(0+)$ and $\frac{d^2i_2}{dt^2}(0+)$

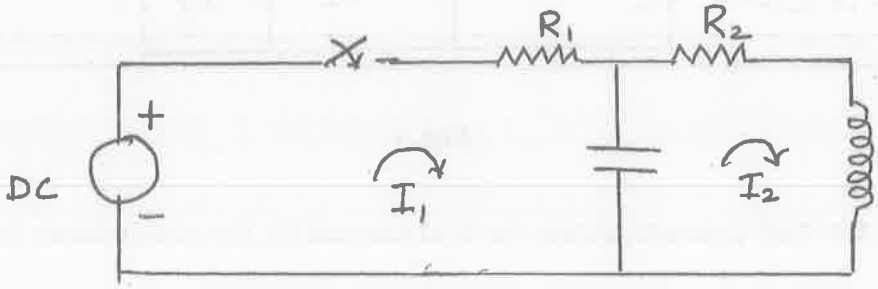


Fig. 10

15. Solve using Laplace Transform method for the following circuit shown in Figure. 11.

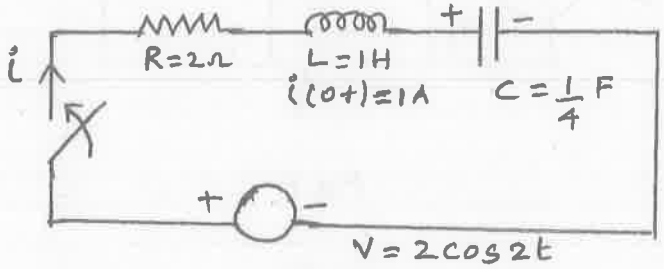


Fig. 11

Or

16. The network shown in Figure (12) reaches a steady state with switch S closed for a long time. At $t = 0$, the switch is opened. Find $i(t)$ for $t > 0$.

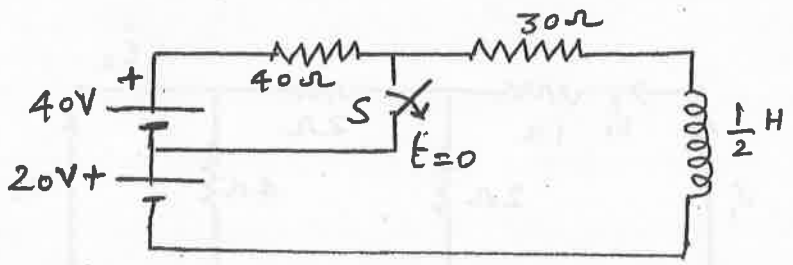


Fig. 12

17. Find the transform impedance of the network shown in Figure 13.

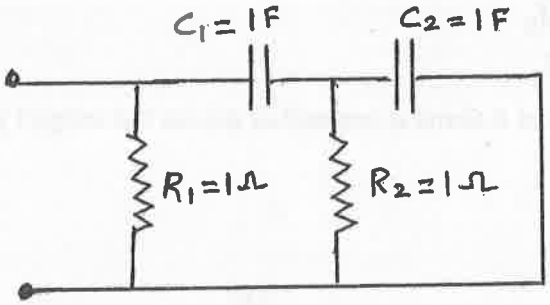


Fig. 13

Or

18. Solve using Superposition Theorem for the following circuit shown in Figure 14.

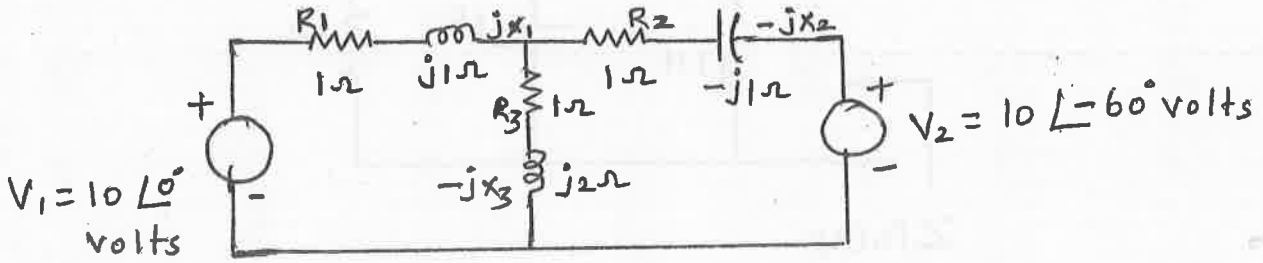


Fig. 14

19. (a) Find the Y parameters for the network shown in Figure 15.

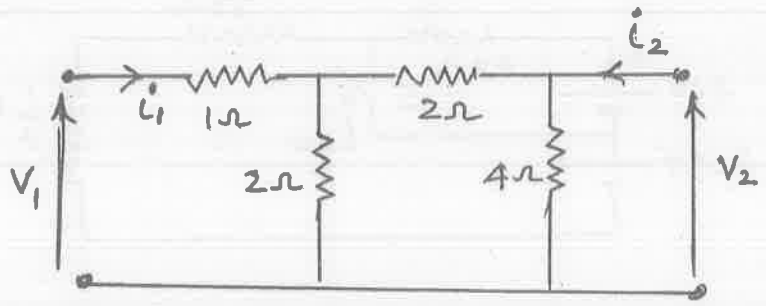


Fig. 15

(6 marks)

(b) The terminal equations of a two - port network are

$V_1 = 5V_2 - 3I_2$

$I_1 = 6V_2 - 2I_2$

A load resistance of 5 ohms is connected across the output port. Determine the driving point input impedance.

(6 marks)

Or

20. Find the driving point impedance function for the network shown in Figure 16 and plot its zero diagram.

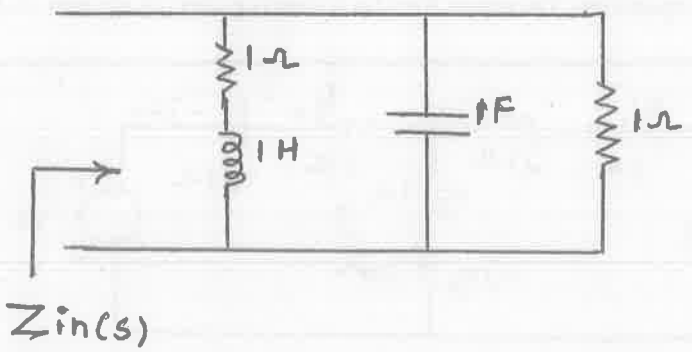


Fig. 16

(5 × 12 = 60 marks)

F 3604 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Third Semester

Branch : Information Technology

DIGITAL ELECTRONICS (T)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. (i) Obtain 2's complement of 01110110.

   (ii) Convert $(101100111)_2$ to gray code.

2. (i) Is the NAND function associative ? Justify.

   (ii) Convert the following Hex decimal number to octal and decimal number : 92FF.7F.

3. Obtain simplified POS using K-map for $f(A, B, C, D) = \Sigma(0, 1, 2, 5, 6, 8)$.

4. Realize a full adder using 2-to-1 MUX.

5. Explain propagation delay, tristate buffer and noise margin.

6. Draw the circuit diagram of a 3-input open collector TTL NAND gate.

7. (i) Sketch the circuit of 1-bit SRAM cell.

   (ii) Convert JK flip-flop into D flip-flop.

8. (i) Distinguish between synchronous and asynchronous sequential circuits.

   (ii) What is race around condition ?

9. Draw a logic diagram of 2-bit ripple counter and convert the same into a 2-bit ring counter.

10. Draw the logic diagram of Universal shift register.

(10 × 4 = 40 marks)

Turn over

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Using a Karnaugh map, determine the MSP and MPS forms of the switching function :

$F = \Sigma m (0, 2, 5, 7, 8, 9, 10, 15) + \Sigma d (3, 4)$.

Or

12. Simplify the following Boolean function using Quine-Mcclusky method :

$F (A, B, C, D) = \Sigma m (0, 2, 3, 6, 7, 8, 10, 12, 13)$.

13. Explain the operation of 4-bit Magnitude comparator.

Or

14. (i) What is the simplest logic for a decoder that produces a '1' output when the BCD input is '0000' ? (6 marks)

(ii) Draw and explain 1-16 De-Mux circuit. (6 marks)

15. (i) Draw the circuit diagram and explain the operation of three input NAND gate using CMOS gate. (6 marks)

(ii) Draw the circuit diagram of CMOS inverter and explain its Operation. (6 marks)

Or

16. (i) With a neat diagram explain the working of tristate TTL gate. (8 marks)

(ii) Analyse the performance characteristics of TTL and CMOS logic. (4 marks)

17. Draw the circuit of a Master-Slave JK FF using NAND gates only and explain its operation for J = K = 1 by assuming an initial value Q = 0.

Or

18. Design a combinational circuit using ROM. The circuit accepts a three bit number and produce outputs a binary number equal to the square of the input number.

19. Design a counter with count sequence 0, 1, 2, 5, 4, 3, 7, 6, 0, 1 and repeat using JK FFs.

Or

20 (i) Consider 4-bit Johnson counter with modification to prevent lock out. Assume the initial state to be 1010. Determine the next states of the counter till a valid state is reached. (6 marks)

(ii) Draw a 4-bit SISO shift register and Explain with its waveforms. (6 marks)

[5 × 12 = 60 marks]

F 3519 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Third Semester

Branch : Common to all Branches

EN 010 302—ECONOMICS AND COMMUNICATION SKILLS

(AI, AN, AU CE, CH, CS, EC, EE, EI, IC, IT, ME, MT, PE, PO, ST)

[New Scheme—2010 Admission onwards]

{Improvement/Supplementary}

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. What are the functions of Commercial banks ?
2. Mention *six* MNC's other than IT field.
3. What is meant by tax evasion system ?
4. Mention the measures to control inflation.
5. What is TRIPS and TRIMS ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Explain the role of Small Scale Industries (S.S.I.).
7. Explain the disadvantages of privatisation.
8. Comment on deficit financing.
9. What is demand pulls and cost push effects of inflation ?
10. Explain the impact of WTO decisions on Indian industry.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Explain the role of RBI in Indian Economy.

Or

12. Comment on the role of stock markets. Briefly explain the problems facing by Indian stock markets.

Turn over

13. Discuss the role of MNC's in Indian Economy.

Or

14. Discuss the future prospects of IT industry in India.

15. Write notes on the following :—

(a) PI. (b) DPI.

(c) GNP.

Or

16. Explain the difficulties in estimating national income.

17. Explain the direct and indirect taxation system of the Ministry of Finance in India.

Or

18. Explain the consiquences and steps to control the tax evasion system.

19. Explain the causes of disequilibrium in India's Balance of Payments (BOP).

Or

20. Explain the importance of General Agreement on Tariff's and Trade (GATT).

(5 × 12 = 60 marks)

F 3560 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Third Semester

Branch : Information Technology

IT 010 305—PRINCIPLES OF COMMUNICATION ENGINEERING (IT)

(New Scheme—2010 Admission onwards)

[Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 3 *marks.*

1. With a block diagram explain TRF receiver.
2. Define AM. Write expression for AM when a $V_c \sin \omega_c t$ carrier is modulated by $V_m \sin \omega_m t$ signal.
3. Define pre-emphasis and state the need for it.
4. Define shot noise. What are its causes ?
5. Sketch the PAM wave if the carrier is 100 kHz square wave and modulating signal is 100 Hz sine wave.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. With neat diagrams explain satellite communication, and discuss its advantages.
7. An audio signal $20 \sin (1200 \pi t)$ is used to amplitude modulate a carrier of $50 \sin \left(2\pi \times 10^5 t\right)$.

   If the modulation index is 0.4, calculate :

   (i) The side-band frequencies. (1 mark)

   (ii) Amplitude of each side-band. (1 mark)

   (iii) Bandwidth. (1 mark)

   (iv) Total power dissipated to load of 600 Ω. (2 marks)

Turn over

8. Find the : (i) Carrier frequency ; (ii) Modulating frequency ; (iii) Modulation index ; and (iv) The maximum deviation of the FM wave represented by the equation $v = 20 \sin \left(8 \times 10^8 \, t + 5 \sin 1000 \, t\right)$.

9. Define and distinguish between SNR and noise figure. What are their significance ?

10. A telephone signal band limited to 4 kHz is transmitted by PCM. The signal to quantization noise is to be at least 40 dB. Find the number of levels into which signal has to be encoded.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. (a) Explain clearly the essentiality of modulation in a communication system. (5 marks)

(b) Describe the electromagnetic spectrum and mention the frequency ranges used for various types of electronic communication.

(7 marks)

Or

12. With a neat block diagram, explain the performance of a double superheterodyne receiver and emphasise the need for the two-level conversion.

13. With neat sketches of frequency spectrum, of the transmitter and receiver sides, explain the VSB system. Clearly explain the correction applied in the receiver side.

Or

14. From fundamentals, derive the expression for the SSB wave containing only the upper side band. Sketch the waveform and spectrum.

15. From fundamentals, derive the expression for the instantaneous value of an FM wave and define the modulation index. Sketch its frequency spectrum.

Or

16. Neatly draw the block diagram of a FM receiver and describe the function of each block.

17. (a) Discuss the sources of internal and external noise. (5 marks)

(b) The noise output of a resistor is amplified by a noiseless amplifier having a gain of 80 and a bandwidth of 20 kHz. A meter connected to the output of the amplifier reads 1 m Vrms :

(i) The bandwidth of the amplifier is reduced to 5 kHz, its gain remaining constant. What does the meter read now ?

(ii) If the resistor is operated at 80° C, what is its resistance ?

(7 marks)

Or

18. (a) Discuss the types, causes and effects of the various forms of noise, which may be created within an amplifier ?

(5 marks)

(b) Discuss the merits of delayed AGC as compared with simple AGC. Show AGC curves to illustrate the comparison and explain how delayed AGC may be obtained and applied ? What does the "delayed AGC control" adjust ?

(7 marks)

19. The signal $g(t) = 10 \cos (30 \pi t) \cos (300 \pi t)$ is sampled at a rate of 400 samples per sec :

(a) Determine the spectrum of the resulting sampled signal.

(b) Specify the cut-off frequency of the ideal reconstruction filter so as to recover $g(t)$ from its sampled version.

(c) What is the Nyquist rate of $g(t)$?

Or

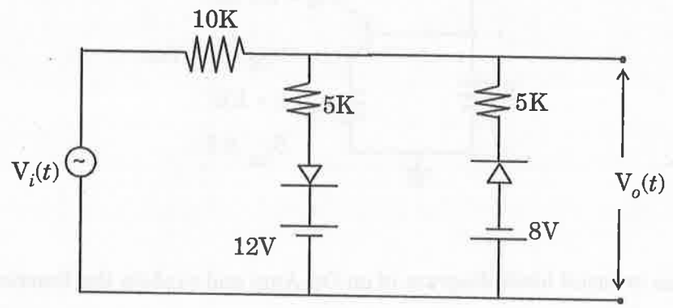
20. Explain the principle of digital PCM ? What is the effect of quantisation ? Bring out the trade-off between bandwidth and signal-to-quantisation noise power ratio.

(5 × 12 = 60 marks)

(b) In a transistorised Hartley oscillator the two inductances are 2 mH and 20 μH while the frequency is to be changed from 950 kHz to 2050 kHz. Calculate the range over which the capacitor is to be varied ? Draw the circuit.

(5 marks)

19. For the circuit shown below, the input voltage is $V_i(t) = 20 \sin 10^4 t$. Sketch the output voltage $V_o(t)$ = for two cycles of sine wave. Assume ideal diodes. Explain the working of the circuit.



Or

20. Design an Op-Amp 741 inverting Schmitt trigger with upper trip point = + 5V, lower trip point = – 4V. Assume that the saturation voltage of 741 is ± 13V for the supply of ± 15V . Derive the equations used.

(5 × 12 = 60 marks)

F 3539 (Pages : 4) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Third Semester

Branch : Information Technology

IT 010 303—DISCRETE AND INTEGRATED ELECTRONIC CIRCUITS (IT)

(New Scheme—2010 Admission onwards)

(Improvement/Supplementary)

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 3 *marks.*

1. Write in which kinds of load conditions the L, C and LC filters are best suited ?
2. Define three stability factors of a CE amplifier.
3. What is the necessity of the level shifter in an Op-Amp ? Which type of circuit is used for it ?
4. State Barkhausen criteria for oscillator ?
5. Draw the circuit of an Op-Amp Schmitt trigger.

(5 × 3 = 15 marks)

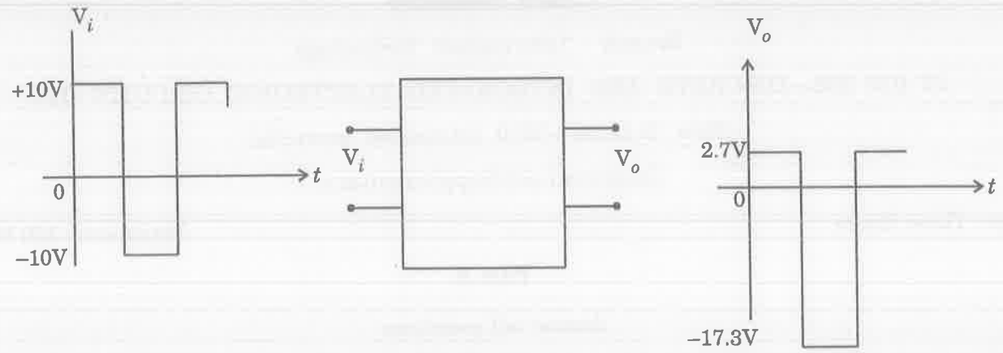
Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. With a neat circuit diagram, explain how a zener shunt voltage regulator is maintaining the output voltage constant, irrespective of changes in (i) line voltage ; and (ii) Load current ?
7. Explain the circuit of collector-to-base feedback bias and explain its special features.
8. Derive the expression for the voltage gain and input resistance of an inverting Op-Amp circuit ?
9. Explain the circuit of Colpitts oscillator and illustrate how sustained oscillations are produced ?

10. Draw a circuit to perform the following function ?



(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. With a neat circuit diagram, explain the voltage regulation in a transistor shunt voltage regulator ? Calculate the values of the resistances in the circuit for getting an output voltage of 6 volt.

Or

12. A single-phase full wave rectifier consists of two diodes each having an internal resistance of 300 Ω. The secondary transformer voltage to centre tap is 280 V. The loaded resistance is 2400 Ω. Calculate.

    (a) The d.c. load current.

    (b) The d.c. current in each diode.

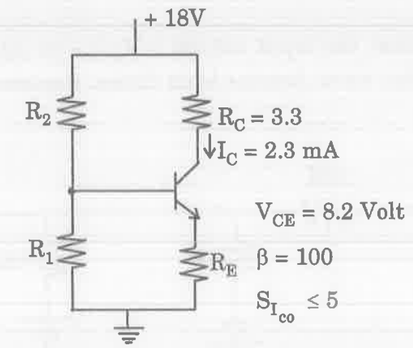
    (c) The a.c. voltage across each diode.

    (d) The d.c. output power.

13. Draw the CE amplifier circuit. Sketch its input and output characteristics and explain the shapes of the curves ?

Or

14. Calculate the values of the resistors in the following circuit.



15. (a) Draw the internal block diagram of an Op-Amp and explain the function of each block in it ? (9 marks)

    (b) Draw the simplified equivalent circuit of an Op-Amp and explain its parameters. (3 marks)

Or

16. (a) Three voltages V_1, V_2 and V_3 are available as outputs from three transducers. It is desired to get output voltage $V_0 = V_1 - V_2 + V_3$. Draw and design the circuit and derive the expression for the output V_0 of the circuit.

(7 marks)

    (b) Draw and design the circuit of an averaging amplifier to find $V_0 = \frac{V_1 + V_2 + V_3}{3}$.

(5 marks)

17. What is a negative feedback ? Show how the input resistance can be increased and the output resistance can be decreased on applying a negative feedback to an amplifier ? Derive the expressions for the above impedances.

Or

18. (a) An amplifier has 60 dB gain. It has an output impedance Z_0 = 10 kΩ. It is required to modify this impedance to 500 Ω by applying negative feedback. Calculate the value of feedback factor. Also find the percentage change in the overall gain, for 10 % change in the gain of the internal basic amplifier.

(7 marks)