G 533 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Information Technology

IT 010 406—OBJECT ORIENTED TECHNIQUES (I T)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Give the features of OOPs.
2. Define class with syntax.
3. What is meant by Inheritance ?
4. Which are the various functions used for unformatted output operations.
5. Which containers use a Border layout as their default layout ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. State different concepts of OOPs. Explain any *two*.
7. State the characteristics of friend function.
8. What is Virtual base class ? Explain with suitable example.
9. What are the steps to be followed while implementing interfaces ?
10. Write short notes on Event listeners.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Explain with suitable example how encapsulation is implemented in C++.

Or

12. Write a program using function to calculate sum of diagonal elements of matrix.

Turn over

13. Write a program to illustrate friend function.

Or

14. Briefly explain overloading of binary operator.

15. Explain the data types available in Java.Explain with example.

Or

16. List out the looping state statements available in Java.Explain with example.

17. Explain in detail about packages.

Or

18. Explain in detail about Multithreading programming.

19. How Applets are prepared and executed ?

Or

20. Write down the comparison of C++ and Java.

(5 × 12 = 60 marks)

G 510 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Computer Science and Engineering/Information Technology

CS 010 403/IT 010 405—DATA STRUCTURES AND ALGORITHMS (CS, IT)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. State the principles of programming ?
2. State any three applications of stack and queue ?
3. What is meant by linked list ? Write down the types of linked list ?
4. Define tree and binary tree.
5. Write the function in C for insertion sort ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. What are the advantages and disadvantages of various collision resolution strategies ?
7. Explain the various applications of stack.
8. Give an algorithm to reverse the elements of a linked list without using temporary list ?
9. Formulate an algorithm to insert an element in a binary tree ?
10. Explain divide and conquer method sorting.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. What is open addressing hashing ? Describe any one technique.

Or

12. Explain in detail about rehashing and extendable hashing.

Turn over

13. Write an algorithm to find whether a particular element is present or not in a circular queue.

Or

14. Implement typical stack operation when stacks are represented using : (a) Arrays ; (b) using singly linked lists ?

15. Discuss the Doubly linked list and algorithm for the operations that can be performed on them in detail.

Or

16. Explain in detail about cursor based linked lists.

17. Explain the various tree traversal and predict a binary tree with Preorder: ABCDEFGHI and Inorder: BCAEDGHFI ?

Or

18. Formulate an algorithm to search an element in a Binary Tree.

19. Write the routine for sorting n elements in increasing order using heap sort.

Or

20. What is external sorting ? Discuss the algorithms with proper examples.

(5 × 12 = 60 marks)

G 521 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Information Technology

IT 010 403—COMPUTER ORGANISATION AND ARCHITECTURE (I T)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Explain the functional components of the computer in detail.
2. Define and explain instruction cycle.
3. Explain the concept of cache memory in detail.
4. What is firewall ? What is its significance ? Explain.
5. Explain the concept and advantages of parallel processing.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Define ALP. Differentiate ALP from High level programming.
7. Explain the organization of a processor with a neat diagram.
8. Explain the features and applications of Semiconductor memories.
9. Give an account on "USB Bus".
10. What is Hazard ? Enumerate the types of Hazard. Explain them.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Discuss the concept of machine level programming in detail.

Or

12. Explain the function and structure of a computer in detail with neat diagrams.

Turn over

13. (i) Explain the design of arithmetic unit with an example.

(ii) Explain the operations of a control unit in detail.

Or

14. Discuss in design of hardware control unit with an example.

15. Explain the structures and applications of SRAM and DRAM cells.

Or

16. Explain the hardware support for memory management.

17. Explain the types of firewall in detail.

Or

18. Write short notes :

(i) Secondary storage devices ;

(ii) SCSI bus ;

(iii) Access of I/O devices.

19. Discuss in detail the design issues of pipeline architecture .

Or

20. Write technical notes on :

(i) Issues of dead lock and scheduling ;

(ii) Synchronization ;

(iii) Multiprocessors.

(5 × 12 = 60 marks)

G 539 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Computer Science and Engineering/Information Technology

CS 010 406/IT 010 404—THEORY OF COMPUTATION (CS, IT)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Define Pigeonhole principle.
2. What are the applications of automata theory ?
3. Define a context free grammar.
4. What is the language accepted by TM ?
5. What does mean SAT ?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Write down the difference between primitive and partial recursive functions ?
7. Differentiate NFA and DFA.
8. What are the applications of pumping lemma ?
9. What are the special features of TM ?
10. Write notes on Reduction problem ?

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each question carries 12 *marks.*

11. Define Diagonalization principle. Prove that the set is uncountable.

Or

12. Explain in detail about the Chomsky classification.

Turn over

13. Conversion of DFA into regular expression.

Or

14. Write notes on deterministic and Non deterministic finite automation ?

15. State and Prove the pumping lemma for CFL.

Or

16. Discuss about deterministic and Non deterministic PDA.

17. Explain the various techniques for Turing machine construction.

Or

18. Prove that the Halting problem is undecidable.

19. Write the characteristic features of *p*-completeness ? Explain with an example.

Or

20. State and Prove Cooks theorem.

(5 × 12 = 60 marks)

G 560 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Information Technology

LINEAR INTEGRATED CIRCUITS AND APPLICATIONS (T)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. What is a level translator ? Where it is used in 741 op-amp ? Explain its role.
2. Define the following op-amp parameters :
   (i) CMRR ; (ii) Bias current ; (iii) Offset current ; and (iv) PSRR.
3. Explain the working of a comparator circuit with necessary waveforms.
4. Describe the characteristics of op-amp notch filter.
5. Explain the following terms for DAC :
   (i) Resolution ; (ii) Settling time ; and (iii) Conversion time.
6. Explain binary weighted D/A converter with a neat circuit diagram.
7. What is the principle of a dual tracking regulator ? Explain.
8. Write a note on general purpose switching regulator.
9. Describe the functional block diagram of a PLL.
10. Explain the principle of LM 380 power amplifier.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Draw the circuit diagram of an instrumentation amplifier using 3 op-amps and derive expression for its overall gain.

Or

Turn over

12. (a) With necessary circuit diagram, explain how output level shifting is achieved in the differential amplifier.

(6 marks)

(b) Explain (i) slew rate ; (ii) input bias current ; and (iii) input offset voltage. (6 marks)

13. (a) Design a second order low-pass Butterworth filter with a – 3 dB frequency of 8.5 kHz. If $V_i(t) = 10 \cos(4\pi \times 10^4 t - 90°)$, find $V_0(t)$.

(8 marks)

(b) In a second order high-pass Butterworth filter, $C_1 = C_2 = 0.047\ \mu F$, $R_3 = R_4 = 2.2$ K, $R_1 = 27$K and $R_F = 15.8$ K. Calculate the lower cut-off frequency.

(4 marks)

Or

14. In a basic triangular-squarewave generator, calculate the component values for a square wave with peak values of ± 5 volt, triangular wave with peak values of ± 10 V, and f_0 continuously variable from 20 Hz to 20 kHz. Draw the circuit and explain its working.

15. Give the circuit of a R-2R ladder network and explain how it can be used as a DAC.

Or

16. With suitable diagrams, explain a successive approximation ADC. Explain its conversion time in terms of clock cycles.

17. Draw the circuit of a linear series pass feedback voltage regulator which uses an overload protection. Explain the working with the help of its regulation characteristics.

Or

18. With a neat circuit diagram, explain how a dual supply ± 9V can be assembled using three pin voltage regulator.

19. Draw and design the circuit of an FM discriminator using 565 to demodulate an FM wave of maximum deviation ± 7% centre frequency 15 kHz, frequency response 200 Hz deviation ratio 5 and $\Delta w = 1044$ Hz.

Or

20. With neat diagrams, describe the functional architecture and working a monolithic waveform generator.

(5 × 12 = 60 marks)

G 570 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, MAY 2014

Fourth Semester

Branch : Information Technology

COMPUTER SYSTEMS ARCHITECTURE (T)

(Old Scheme—Prior to 2010 Admissions)

[Supplementary/Mercy Chance]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Give the details of the hardware interrupts in 8085.
2. Draw and describe the timing diagram for the execution of MOVE, A.
3. Explain clearly any *two* stack instructions.
4. What are the different control and status signals of 8085 ? Explain their functioning.
5. Illustrate any *one* technique for speeding up the multiplication process.
6. Explain signed division operation with an example.
7. Define (i) hit rate ; (ii) miss rate ; (iii) miss penalty ; and (iv) capacity miss.
8. Discuss the concept of memory interleaving and give its advantages.
9. With a neat diagram, explain asynchronous handshaking protocol to read a word from memory and receive it in an I/O device.
10. Compare and contrast programmed I/O with interrupt driven I/O.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. (a) Explain a method for latching low-order address bus of 8085. Also give the details of different flags available in 8085.

    (b) If [HL] = 2005 and [A] = 03, what are the contents of the location 2005 after execution of MOV M, A and STA 2005 instructions.

Or

Turn over

12. Draw the timing diagram of an opcode fetch machine cycle of 8085 with one wait state and the different status and control signals. Explain.

13. Classify the instruction set of 8085 in various groups and give at least three examples of instructions for each group.

Or

14. Describe the various I/O and machine control group instructions and data transfer instructions in 8085, with appropriate examples.

15. Make a comparative study in terms of cost of number of logic gates and speed of 4 different n-bit adders-ripple carry, carry look ahead single level, carry look ahead two level and carry save adder.

Or

16. Multiply the following pair of signed 2's complement numbers using the Booth algorithm :

    A = 010111 (multiplicand)

    B = 110110 (multiplier)

17. Compare direct mapping, set associative and fully set associative cache and explain cache misses in each case by taking suitable examples.

Or

18. What is virtual memory ? Explain how virtual addresses are mapped to physical address.

19. Explain the following data transfer schemes and their applications :

    (i) DMA data transfer.

    (ii) Interrupt driven data transfer.

Or

20. Explain clearly (i) SCSI bus architecture ; and (ii) GPIB bus standard.

(5 × 12 = 60 marks)