F 3615 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Fifth Semester

Branch : Information Technology

IT 010 502 – MICROPROCESSORS AND MICROCONTROLLERS [IT]

(New Scheme – 2010 Admission onwards)

[Regular / Improvement / Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*

Each question carries 3 *marks.*

1. What is the need for MN/M $\overline{X}$ pin on 8086 microprocessor?
2. Explain the use of PUSH and POP instructions in 8086.
3. What do you mean by BSR mode of 8255 PPI?
4. What are the flags available in 8051?
5. How does 8051 differentiate between external and internal program memory?

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*

Each question carries 5 *marks.*

6. Draw the timing diagram for I/O read operation and explain.
7. Write a short note on Macros.
8. Explain the input modes provided by 8279.
9. Compare and contrast microprocessors and microcontrollers.
10. Explain the interrupt structure of 8051.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*

Each full question carries 12 *marks.*

11. Explain the register organisation of 8086. Also explain the purpose of each registers.

(12 marks)

Or

12. (i) Explain the pipelining structure of 8086.

    (ii) Explain with example, how physical address is formed in 8086.

(6 + 6 = 12 marks)

Turn over

13. (i) Explain the steps assembler follows to convert .ASM file and .OBJ file.

(ii) Differentiate between machine language and assembly language.

(7 + 5 = 12 marks)

Or

14. Draw and explain the interrupt structure of 8086.

15. Draw and discuss the internal architecture of 8257.

Or

16. With a neat architecture, explain the model of 8253.

17. Write a program in 8051 to convert a given 8-bit binary number to its Grey code equivalent.

Or

18. Draw and discuss the internal diagram of 8051 microcontroller.

19. Explain the timer/counter functional unit of microcontroller 8051 with relevant diagrams.

Or

20. Write an ALP for interfacing 8051 with matrix keyboards.

(5 × 12 = 60 marks)

F 3704 (Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Fifth Semester

Branch : Information Technology

MICROPROCESSORS (T)

(Old Scheme—Supplementary/Mercy Chance)

[Prior to 2010 Admissions]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 4 *marks.*

1. Explain logical and physical address of 8086 microprocessor with example.
2. Explain stack memory addressing modes of 8086 microprocessor.
3. Explain data transfer concepts in 8086 microprocessor.
4. Write down the different types of assembler directives of 8086. Explain any *two* in detail.
5. Draw the timing diagram of memory READ operation in 8086.
6. Give the logical circuit for memory read, write and IO read, write signal derived from 8086.
7. What is the purpose of debug and test registers of 80386 microprocessor ?
8. Illustrate the format of a flag register of 80286 microprocessor.
9. Explain the format of I/O mode set control word of 8255.
10. Explain a status word format of 8279 programmable keyboard and display interface.

(10 × 4 = 40 marks)

Part B

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. With a neat sketch explain the internal architecture of 8086 microprocessor.

Or

12. (a) Explain the memory organization of 8086 microprocessor. (6 marks)

    (b) Illustrate segmented memory and physical address calculation of 8086 microprocessor. (6 marks)

Turn over

13. Explain the various types of instruction set of 8086 with an example.

Or

14. Write an assembly language program using 8086 instructions to find the largest number in a block of data stored in the memory locations from 60 H to 6 FH.

15. (a) Draw and explain the read and write cycle timing diagrams of 8086 in minimum mode. (6 marks)

(b) Discuss the address decoding process of 8086 microprocessor. (6 marks)

Or

16. (a) How will you interface two 4 K × 8 ROM and two 4 K × 8 RAM chips with 8086. Select suitable maps ? (6 marks)

(b) Specify the signals of 8086 used in maximum mode. Explain the function of each of them. (6 marks)

17. Discuss the real and protected modes of operation of Pentium IV. Also illustrate memory paging done in virtual mode ?

Or

18. With a neat sketch explain the architecture of 80286 micro processor.

19. With a neat functional block diagram explain the functions of 8279 keyboard controller.

Or

20. With a neat block diagram describe how a stepper motor is interfaced with 8086 microprocessor.

(5 × 12 = 60 marks)

(Pages : 2) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Fifth Semester

Branch : Information Technology

IT 010 503—DATA COMMUNICATION (IT)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

What is the concept of FDDI ? Explain.

What is the principle and need for multiplexing ?

Mention the features and applications of asynchronous data transmission.

Name a transmission line that can be used in UHF range. Justify your answer.

What is the concept of SDMA ? Explain in detail.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

Explain the principle of wireless LAN with a neat diagram.

State and explain Shannon's theorem.

Define and explain noise. Enumerate the types of noise.

Drawa twisted pair cable and explain its construction and applications.

Discussthe security issues in Data communication.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

(i) Explain the components of Data communication in detail.

(ii) Explain OSI model with a neat diagram.

Or

(i) Explain the network topologies in data communication.

(ii) Give an account on "Ethernet".

Turn over

13. (i) Draw a neat block diagram of TDM and explain its principle in detail.

(ii) Define and explain Channel capacity. Derive an expression for Channel capacity.

Or

14. (i) What is OOK modulation ? Explain with neat diagrams.

(ii) Compare and contrast ASK and FSK.

15. (i) Explain the concept of Half duplex and full duplex with neat diagrams.

(ii) Give an account on "Characteristics of fiber optic cable".

Or

16. Discuss the components of computer communication with diagrams.

17. (i) Discuss the different types of noise in detail.

(ii) Differentiate circuit switching from packet switching.

Or

18. (i) Explain the characteristics of co axial cable in detail.

(ii) Write a technical note on "DSL modems ".

19. (i) Explain the concept of TDMA with a neat diagram.

(ii) Explain the architecture of GSM with diagrams.

Or

20. (i) Draw and explain FDMA frame structure in GSM.

(ii) Write a technical note on "Connection establishment".

(5 × 12 = 60 marks)

F 3671 (Pages : 3) Reg. No.....

Name.....

B.TECH. DEGREE EXAMINATION, NOVEMBER 2016

Fifth Semester

Branch : Information Technology

IT 010 505—LANGUAGE TRANSLATORS (IT)

(New Scheme—2010 Admission onwards)

[Regular/Improvement/Supplementary]

Time : Three Hours Maximum : 100 Marks

Part A

Answer **all** *questions.*
Each question carries 3 *marks.*

1. Differentiate linkers and loaders.
2. What is the role of syntax analysis in compilation ?
3. Compare inherited and synthesized attributes.
4. Define a basic block. Give an example.
5. List the various sources of optimization.

(5 × 3 = 15 marks)

Part B

Answer **all** *questions.*
Each question carries 5 *marks.*

6. Explain the role of lexical analysis.
7. Write rules for finding FIRST and FOLLOW sets for a given CFG. Find FIRST and FOLLOW sets of the symbols in the following grammar :

   $E \rightarrow TA.$
   $A \rightarrow +TA/E.$
   $T \rightarrow FB.$
   $B \rightarrow *FB/E.$
   $F \rightarrow (E) / id.$

8. Discuss the different parameter passing methods with example.

Turn over

9. Construct the Directed Acyclic Graph (DAG) for the following basic block :

$d = b * c.$
$c = d + b.$
$b = b * c.$
$a = c - d.$

10. What do you mean by peephole optimization ? Explain.

(5 × 5 = 25 marks)

Part C

Answer **all** *questions.*
Each full question carries 12 *marks.*

11. Explain the various phases of a compiler. Show the output of each phase for the following source language statement :

$y = a * b + a * b.$

Or

12. Write notes on :

(i) Interpreter.

(ii) Assembler.

(iii) Incremental compiler.

(iv) Bootstrap compiler

13. Construct the sets of LR (0) items and the SLR parsing table for the grammar :

$F \rightarrow id(P);$
$P \rightarrow P \& id/id.$

Or

14. Write the algorithm for construction of predictive parser. Using the algorithm construct a predictive parser for the following grammar :

$S \rightarrow (L) / a$
$L \rightarrow L, S/S$

15. Compare and contrast different storage allocation strategies used in run time environments.

Or

16. Explain top down and bottom up evaluation of attributes with an example.

17. Construct quadruples, triples and indirect triples for the following expression :

$a = (a + b) * (c + d)$

Or

18. What is a flow graph ? Explain how a given program can be converted into flow graph.

19. Write the algorithm of a simple code generator. Using the algorithm generate code for $w = (x + z) - (x - y)$.

Or

20. Explain global data flow analysis with an example.

(5 × 12 = 60 marks)